Advanced MEMS and Microsystems

Dr. Danick Briand, Prof. Guillermo Villanueva

Announcements

TODAY 06 May 2025

- Lecture on MEMS Packaging

NEXT WEEK 13 May 2025

- Seminar 5 – CSEM at 10h15
- Lecture on MEMS Packaging until 12h

WEEK AFTER 20 May 2025

- Lecture on PowerMEMS (2h) LAST SESSION / No Class on 27.05
- Seminar 6 – Melexis at 12h15

Course content

Dates	Topics	Lecturers
18.02	Introduction Transducers review: pre-recorded lectures	D. Briand / G. Villanueva
25.02	Sensors part I Exercices	D. Briand
04.03	Sensors part II Industrial seminar #1	D. Briand
11.03	Students presentations	D. Briand / G. Villanueva
18.03	Actuators and Optical MEMS Industrial seminar #2	D. Briand
25.03	Acoustic and Ultrasonic MEMS Industrial seminar #3	G. Villanueva
01.04	RF-MEMS	G. Villanueva
08.04	NEMS	G. Villanueva
15.04	Interactive session	D. Briand / G. Villanueva
29.04	Thermal and gas sensors Industrial seminar #4	D. Briand
06.05	Packaging	D. Briand
13.05	Packaging Industrial seminar #5	D. Briand
20.05	PowerMEMS Industrial seminar #6	D. Briand
27.05	Quiz + oral exam instructions Evaluation of the course **NO CLASS**	All

LESSON 8 – Packaging

Dr. Danick Briand

Maître d'Enseignement et de Recherche (MER)

Team leader MEMS & Printed Microsystems

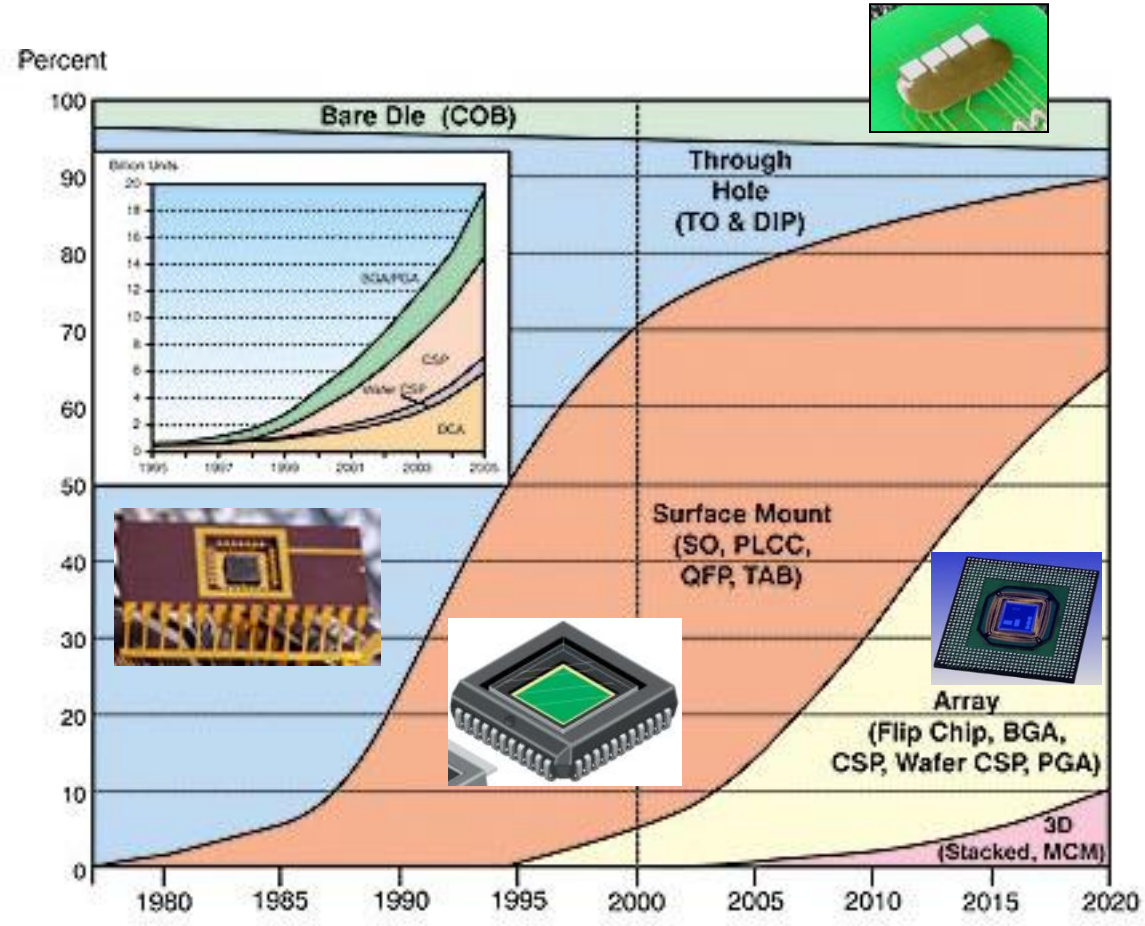
EPFL-STI-LMTS

Contents

- Introduction to packaging
- Overview of bonding techniques for packaging
- Packaging for the integrated circuits
- Specific packaging for Microsystems
- Hermetic packaging
- 3D Integration

Introduction to packaging

Packaging in the IC industry



COB: Chip On Board
DIP: Dual In Line Package
SO: Small Outline
PLCC: Plastic Leaded Chip Carrier
QFP: Quad Flat Pack
TAB: Tape automatic bonding
Flip Chip: Chip turned upside down
BGA: Ball Grid Array
CSP: Stacked Chip-Scale Package
WLP: Wafer level packaging
PGA: Pin Grid Array
MCM: Multi Chip Module

LTCC: Low Temperature Co-Fired Ceramics
HTCC: High-Temperature Co-fired Ceramic
PCTF: Plated Copper on Thick films

Trend is to 3D (vertical stacking), to System in Package and to arrays due to increasing density and number of connections, and need for high speed interconnections between chips.

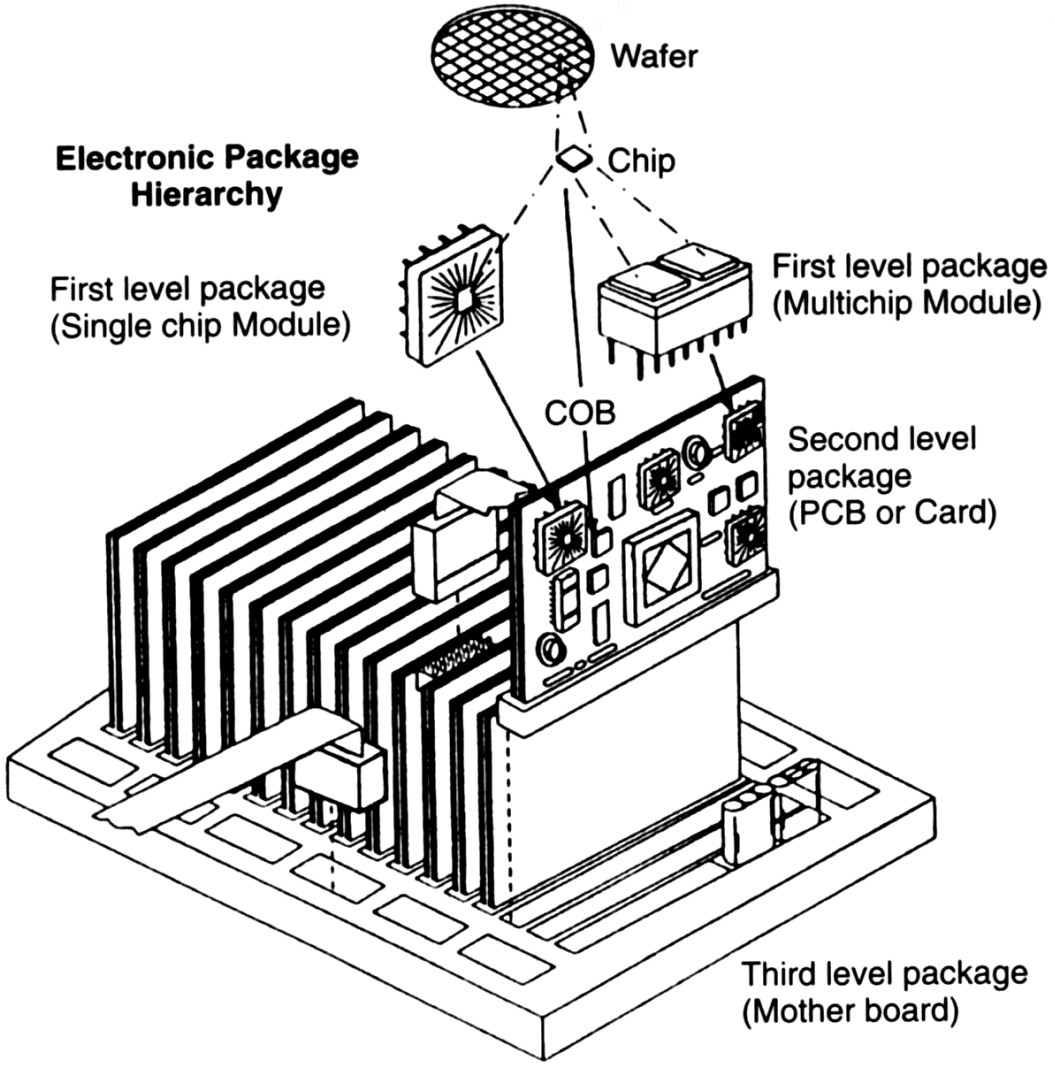
http://www.chipscalereview.com/issues/0701/f4_01.html

Packaging levels microelectronics

Several levels of packaging:

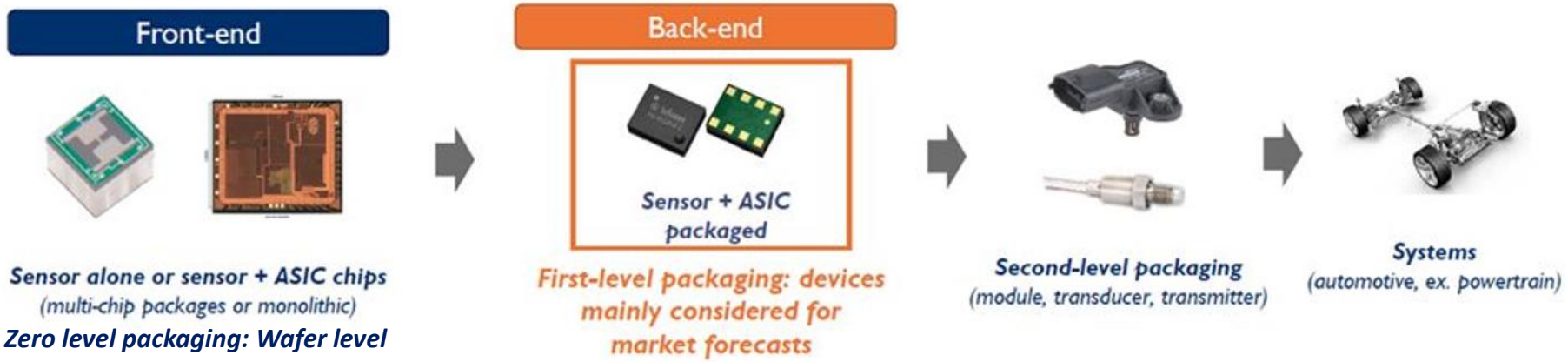
- **Level 0: Wafer level only used on MEMS (for microelectronics can just cover everything except the bond pads with oxide or polymer)**
- **Level 1: Chip level (single or multi-chip module): chip to package or chip to board**
- **Level 2: PCB or Card: package to PCB**
- **Level 3: motherboard: card to card**

PCB: Printed Circuit Board



From J.H. Lau, ed., *Flip-Chip Technologies*, McGraw Hill, NY 1996

Packaging levels MEMS

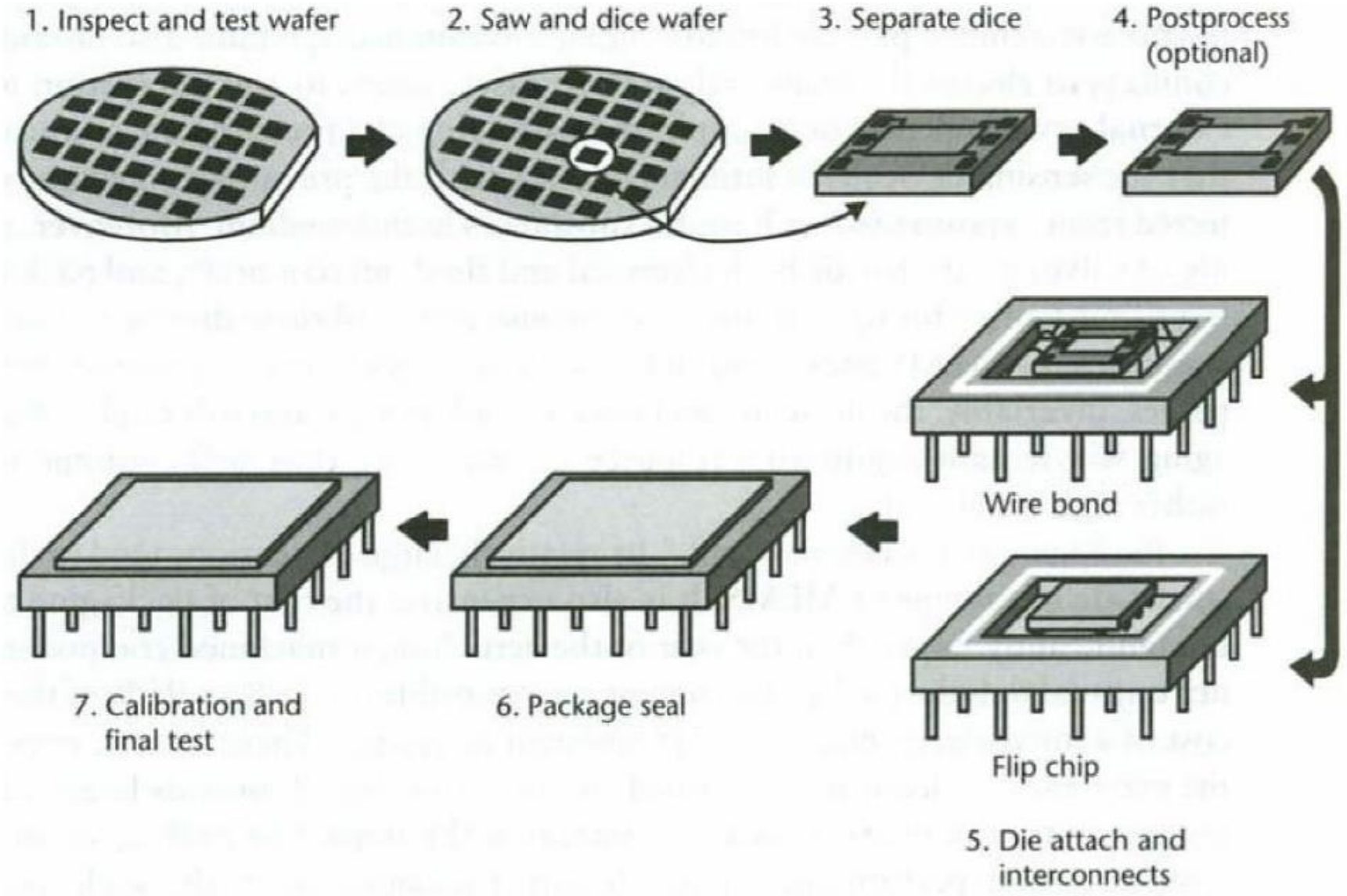


Roles of a package:

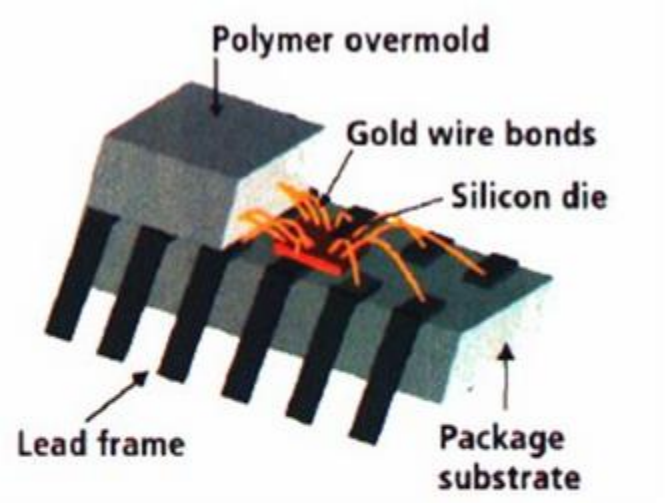
1. **Physical support**
2. **Physical interface**
3. **Electrical connections** (power & signal)
4. **Thermal** (heat transfer)
5. **Protect against the environment** (humidity, corrosion, contamination, gas, liquids, shock, vibrations, electric fields)
6. **Provide controlled working environment** (ex. accelerometer, gyro)
7. **Provide interaction with external environment for actuators** (light, fluid…)
8. **Provide access for the physical or chemical stimuli** (for sensors)

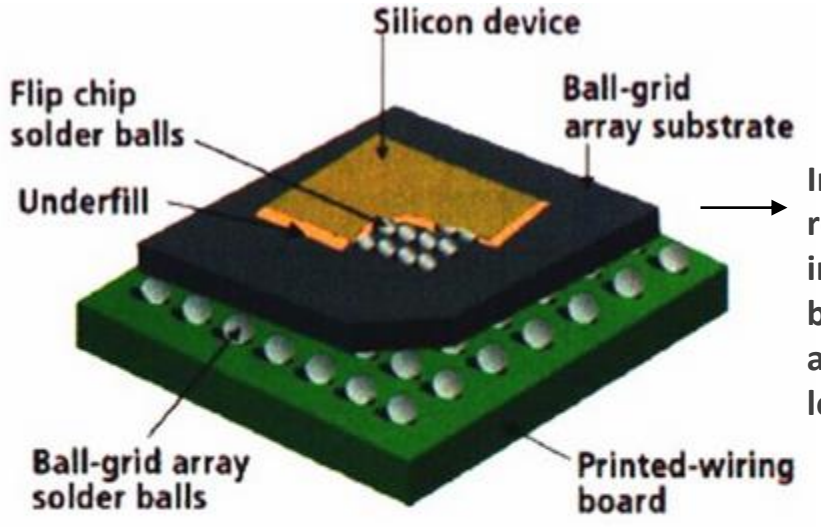
In blue: specific to MEMS devices

Main packaging steps



Main packaging steps





Interposer to reroute the interconnections between IC chip and PCB (high to lower density)

wire-bond plastic DIL pkg

DIL: Dual-in-Line

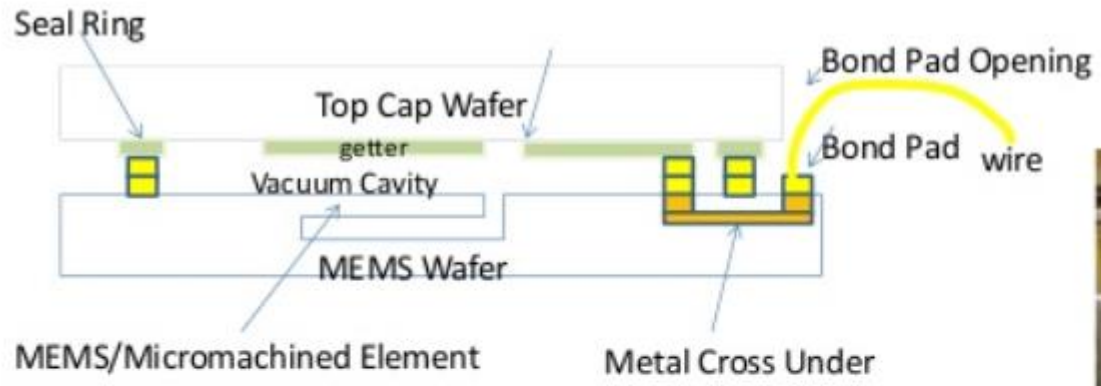
flip-chip BGA pkg

Ball Grid Array

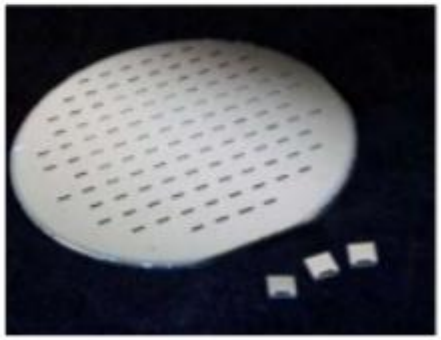
Underfill: Polymeric resist flowing well between chip and substrate used for mechanical fixation

Wafer level packaging (WLP)

- Encapsulation of MEMS at the wafer level, before dicing the chips
- Involve normally wafer bonding of a “cap” wafer



Bonded wafers + WLP dies



Wafer to Wafer Alignment not just bonding

Main packaging steps

Typical steps:

0. Wafer level packaging if applied
1. Wafer level testing / burn-in
2. Dicing (singulation)
3. Die attach: mechanical contact
4. Electrical contact: wire bonding, flip-chip + soldering …
5. Encapsulatation of wirebonds, polymer underfill if flip-chip for mechanical stability of the assembly
6. Final test, burn-in, ship

MEMS packaging

Techniques from IC-industry have been adopted with specific processes for hermetic bonding.

- However **MEMS require** access to outside world

- MEMS-packaging is more complicated than IC-packaging
  - Each MEMS application has unique requirements (high diversity)
  - MEMS packaging often specialized for the application
  - Devices may be fragile

- Little standard exists (often proprietary, one MEMS: one package)

→**Design of MEMS and packaging is highly interconnected**

MEMS packaging: Important considerations

- Thermal: thermal budget, stability, CTE miss-match, conductivity & dissipation, …
- Mechanical Stress (including long term drift)
- Calibration and Testing
- High yield
- Reliability
- Cost: can go up to 75 to 95 % of total cost

*CTE: Coefficient of Thermal Expansion

Major issues in MEMS packaging

- Die handling and dicing
- Stress
- Outgassing
- Encapsulation / hermetic seal (long term)
- Integration
- Reliability
- Testing
- Media compatibility
- Access to the stimuli from the environment (light, gas, liquid…)
- Modularity
- Often package must be designed specifically for device
- Small quantities
- Can easily reach 75% of total cost

Overview of bonding techniques for packaging

Wafer bonding

- **Direct bonding involves bare or oxidised Si and glass wafers**
  - It results in strong chemical bonds across the bonding interface
  - Breakage happens inside the wafers and not at the bond interface
  - Wafer can be processed as if they were one wafer

- **Indirect bonding uses a great variety of materials as « adhesive layers / glues »: metals, glass and polymers**

- **Bonding methods differ mostly in their temperature range and permanency**
  - Direct bonding is usually hermetic and permanent, when performed at high temperature
  - Bonding with intermediate layers is done at lower temperature (<500°C) and it may or may not form a hermetic seal. The intermediate layer limits the process temperature and ambients.

Wafer bonding

- **The driving force for bonding can be temperature, pressure, electric field or a combination of these**

• Fusion bonding (FB)	Si/Si, SiO_2/Si, glass/glass
• Anodic bonding (AB)	Si/glass, glass/Si/glass
• Thermo-compression bonding (TCB)	Si/glass frit; metal/metal
• Adhesive bonding	Si/polymer/Si

- **Fusion bonding temperature range is up to 1200°C for silicon and quartz, and about 600°C for glasses**
- **Anodic bonding and TCB are performed typically in the range of 300 to 500°C**
- **Adhesive bonding below 200°C**

Wafer bonding

- **Basic requirements for good wafer bonding are:**
  - **The materials being bonded form a chemical bond across the interface**
  - **High stress are avoided (CTE matching between the materials)**
  - **No interface bubble / voids formation during the bonding**

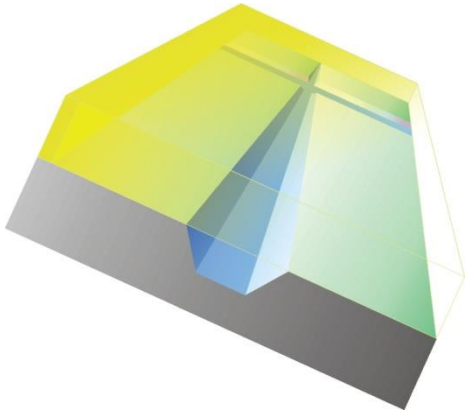
- **Typical bonding steps:**
  - **Surface cleaning**
    - **Particle removal**
    - **Hydrophilic surface finish treatment**
  - **Room temperature joining (aligment if structured wafers)**
    - **Initiation of bonding at the centre or wafer flat**
  - **Anneal for bond energy improvement**

Silicon-glass anodic bonding

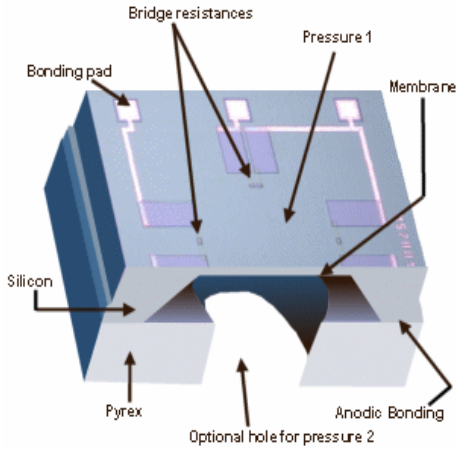
- **Field assisted thermal bonding**
- **Heating at 350-450°C**
  - CTE match is important (Corning 7740 Pyrex, Schott 8339)
- **-300 to -1000 V applied to the glass**
  - When glass is heated up sodium oxide, Na_2O, decomposes into sodium and oxygen ions
  - Due to the electrical field, the sodium ions (Na^+) move towards the glass top surface and oxygens ions (O_2^-) towards the Si
  - This creates an electrostatic field (E=500MV/m) and a strong electrostatic force (that pulls the two wafers together)
  - Oxygen ions react at the glass/silicon interface according to

    $Si + 2O^{2-} \Rightarrow SiO_2 + 4e^-$
  - Sodium ions are neutralised at the cathode
  - Higher temperature, quicker diffusion of Na, larger depletion region = stronger bond
  - Current is monitored and decreases with the formation of SiO_2

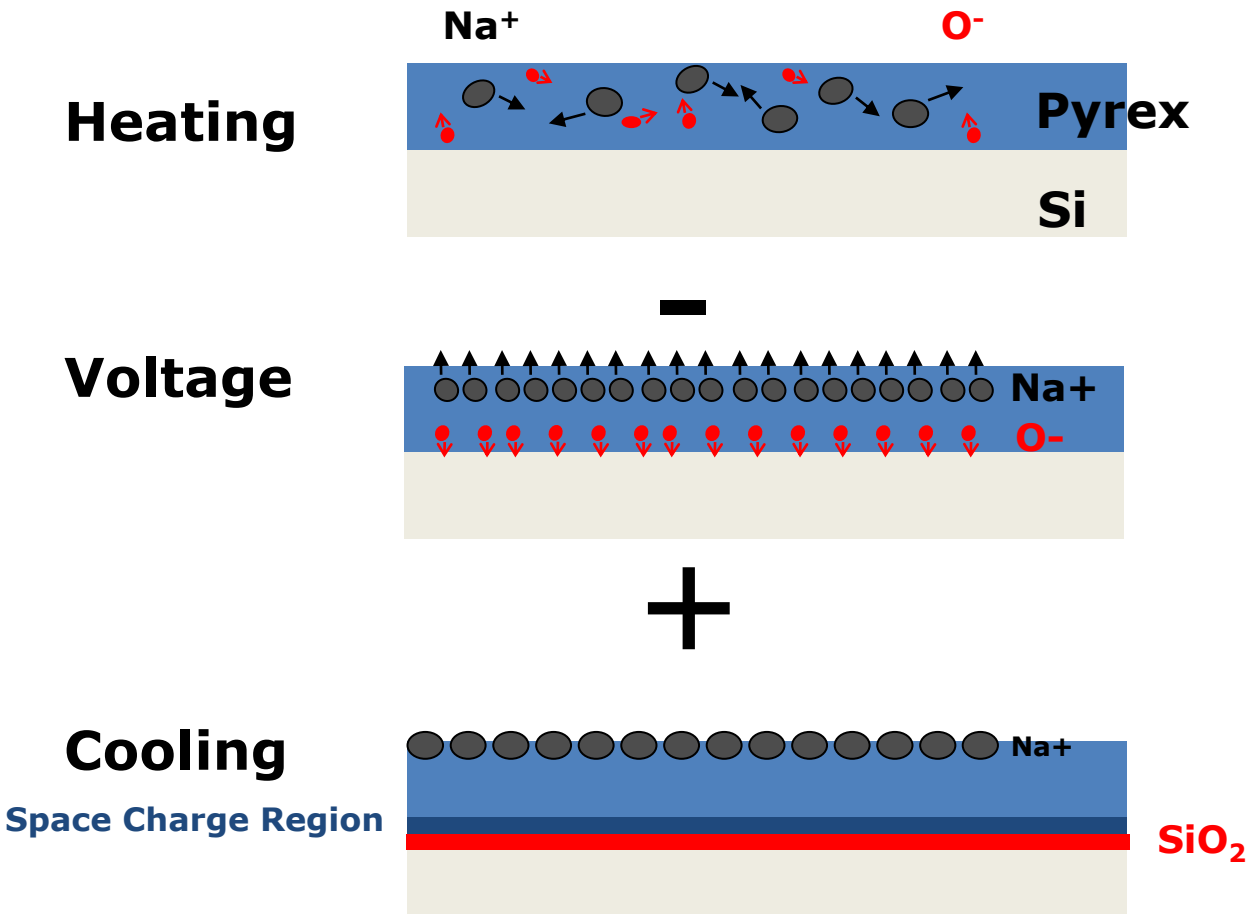
Silicon glass channels



Si Pressure sensor with glass support



Silicon-glass anodic bonding



In situ investigation of ion drift processes in glass during anodic bonding

B. Schmidt [a,*], P. Nitzsche [a], K. Lange [a,1], S. Grigull [a], U. Kreissig [a], B. Thomas [b], K. Herzog [b]

[a] *Forschungszentrum Rossendorf, Institut für Ionenstrahlphysik und Materialforschung, Postfach 510119, D-01314 Dresden, Germany*

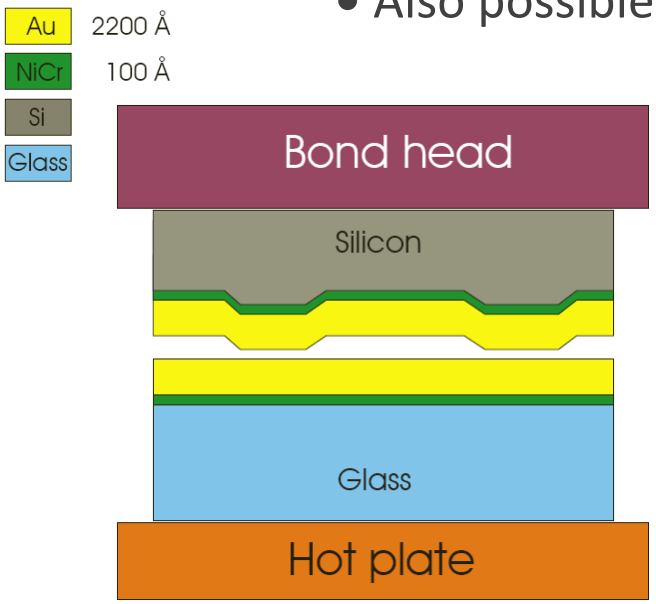
[b] *Institut für Analytische Chemie, TU Bergakademie Freiberg, D-09596 Freiberg, Germany*

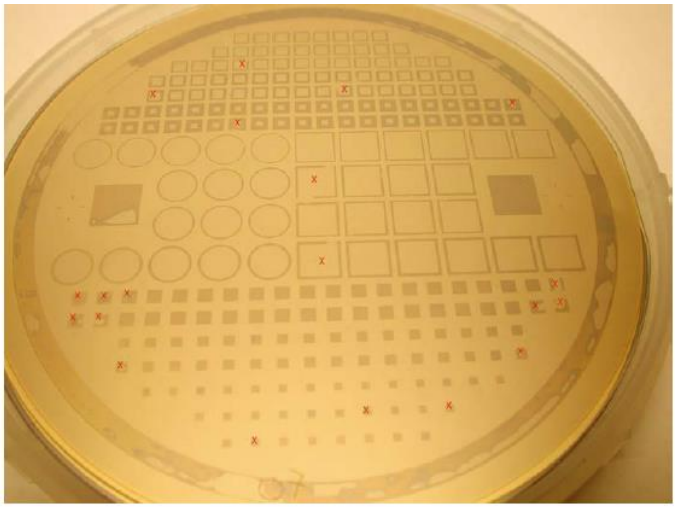
Silicon-glass anodic bonding

- CMOS compatible temperature, but electric field can be problematic
- Bonding Glass/Si/glass stack is possible
- Possible to bond to silicon wafers with intermediate sputtered pyrex glass films
- Bonding of borosilicate glass on thick polysilicon films, rims can be patterned to cover the steps on the chip
- Possible to bond two glass wafers together with an intermediate polysilicon or amorphous silicon film
- Metal to glass anodic bonding possible (limited choice of metals due to CTE)

Thermo-compression bonding (TCB)

- **Application of pressure and heat simultanously on the samples**
- **Standard technique to attach gold leads to ICs**
- **Gold is normally used: Noble metal and no gold oxides on the surface**
- **Wafer level TCB, Pressure of 1 to 10 MPa, 300-400°C with N_2**
- **Wafer bonding possible using thin Au films on both wafers**
  - Also possible Cu, Al, In at lower temperatures



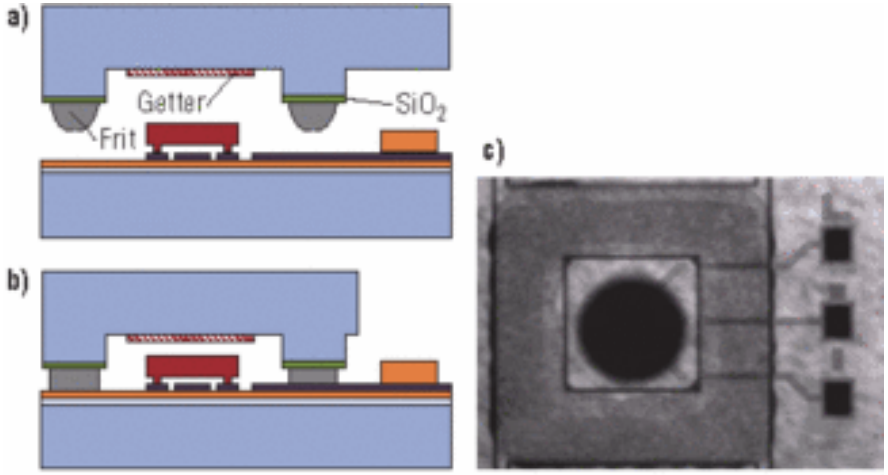


Stack M (~340 °C, 4 MPa)

From SINTEF, Norway

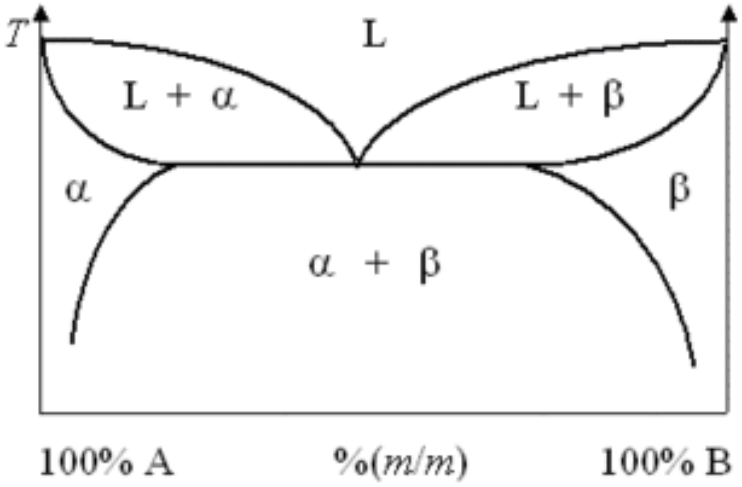
Glass frit

- Also part of the TCB family
- Glass paste doped with ions for a low glass transition temperature
- Certain glass melt under pressure at 500°C and form hermetic bond
- Glass lines with thickness of few microns can be patterned by screen-printing locally on the wafers/chips
- Good technique to cover the steps (metallic interconnections) on the wafer compared to anodic bonding, also more versatile, less dependant on the materials covering the wafers



Soldering and eutectic bonding

- Soldering is a process in which two or more metal items are joined together by melting and flowing a filler metal, the filler metal having a relatively low melting point. Soft soldering is characterized by the melting point of the filler metal, which is below 400 °C. The filler metal used in the process is called solder.
- The melting point of a mixture of two or more solids (such as an alloy) depends on the relative proportions of its ingredients. A eutectic or eutectic mixture is a mixture at such proportions that the melting point is as low as possible, and that furthermore all the constituents crystallize simultaneously at this temperature from molten liquid solution.
- **Solders: Sn-Pb** (63/37)**, Au-Sn** (80/20)**, Sn-Ag-Cu: SAC** (95%+/3-4%/0.5–0.7%)
  - Melting from 150 to 250°C
  - Bumps electrodeposited on Au or Cu pads (UBM=underbump metals on Al pads)
  - Screen printed, sputtered or evaporated
  - Flux (reducing agent) used to avoid oxidation
    - Outgassing problematic for vacuum packaging
- **Eutectic soldering: Au film in contact with Si**
  - Eutectic formation at 370°C
- **CMOS compatible temperatures**



Adhesive bonding

- **Polymers materials are soft materials and they conform to particles, and there will be less problems with voids**
- **Main problems, limited long-term stability and limited thermal range, 400°C the maximum, for most of them 200°C and below**
- **Low temperatures and « soft process », can be CMOS compatible**

Typical steps in adhesive bonding:

- Surface cleaning and adhesion promoter application
- Spin coating of polymer
- Initial curing (solvent bake)
- Join the wafers (vacuum may be used to avoid bubbles)
- Final curing of the polymer; pressure and/or heat

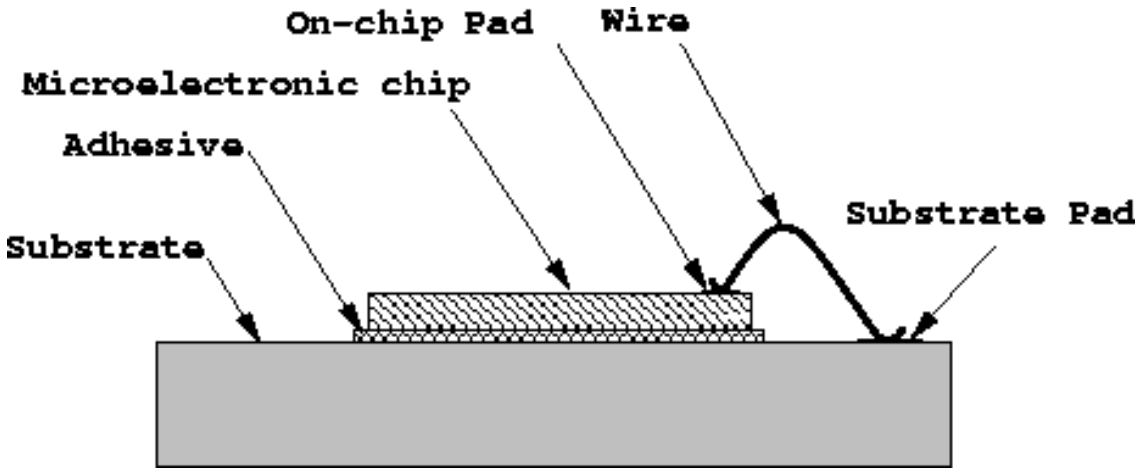
Adhesive glues, films, and spin coatable films

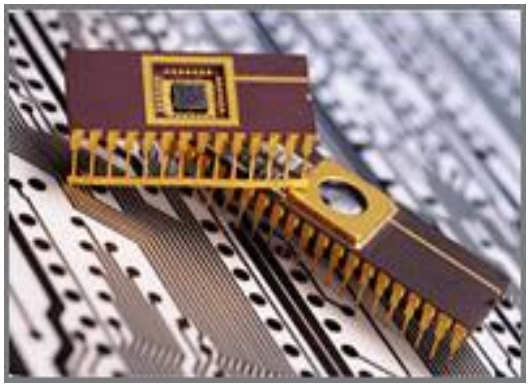
- Epoxy and acrylic glues
- UV curable glues
- Spinable adhesive films
  - Waferbond®, Aquabond®, …
- Spinable films with specific bonding processes:
  - PDMS, PMMA, SU-8, photoresist
  - BCB (Benzocyclobuten with low-k)
  - CYTOP-Fluoropolymer, …
- Electrically conductive materials also available
  - Isotropic conductive adhesive (ICA)
  - Anisotropic conductive adhesive (ACA), films (ACF)

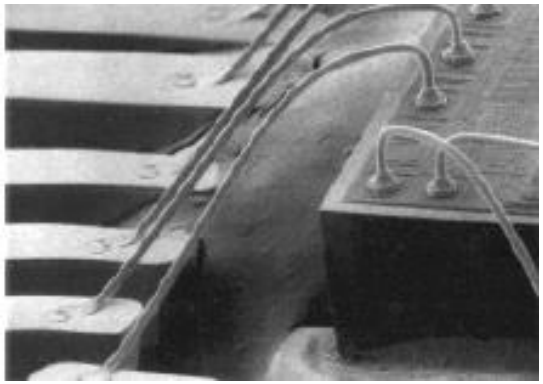
Packaging for Integrated Circuits (ICs)

Through hole package

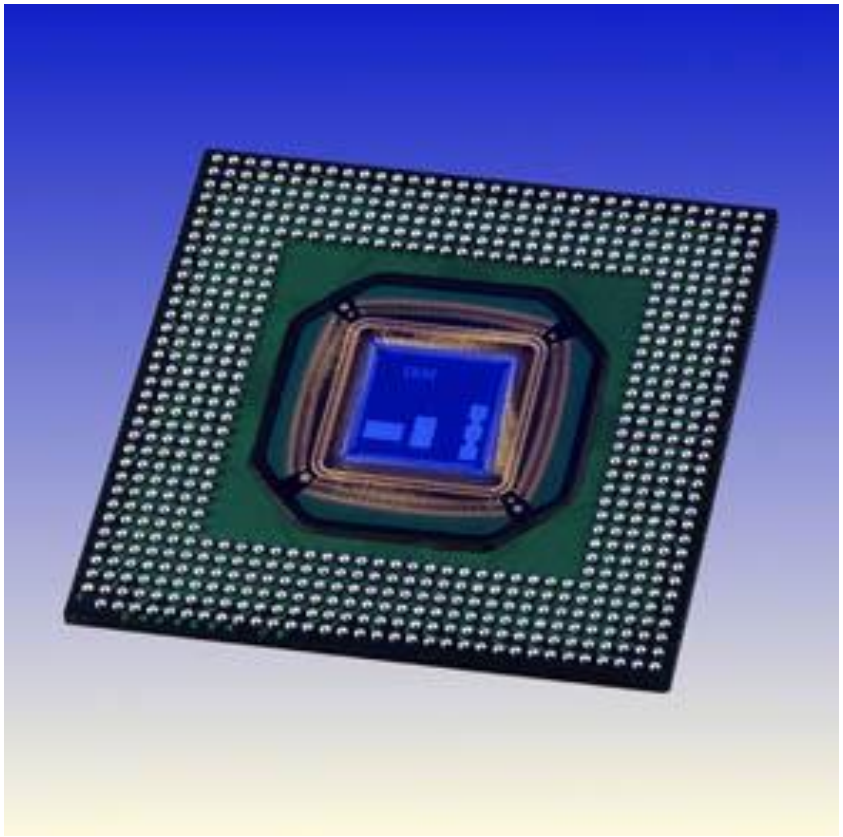
- Gluing the chip in a Dual in Line Package (DIL)
- Wire bonding: typically 25 µm wide gold wire to Al bond pads





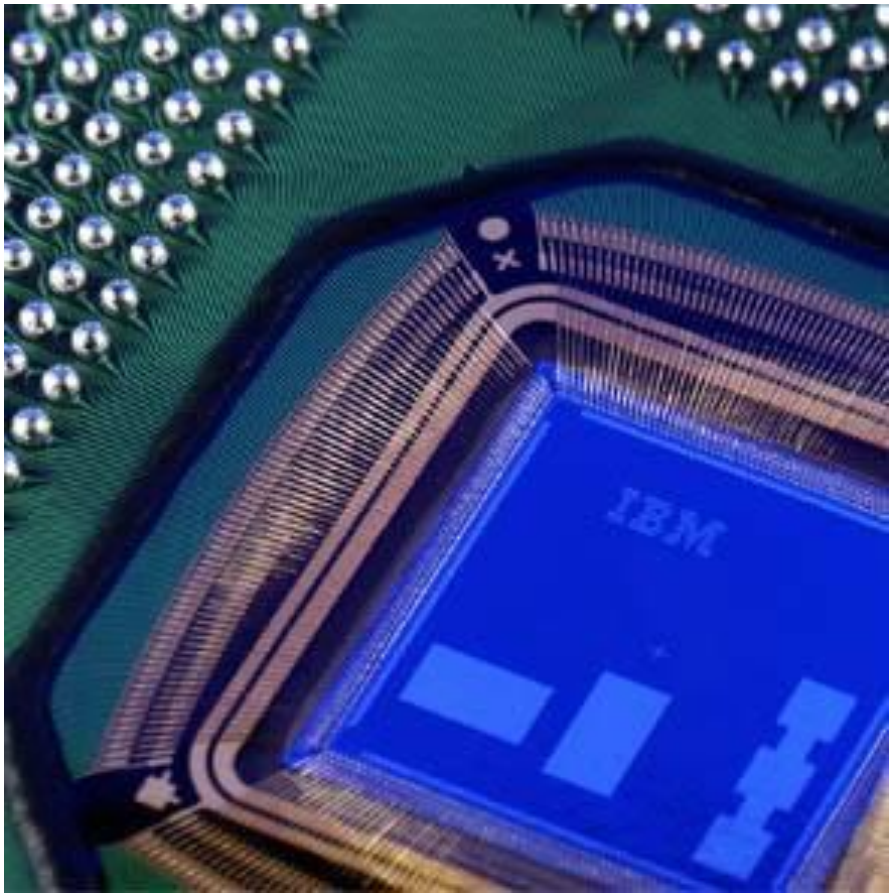


Ball Grid Array (BGA)

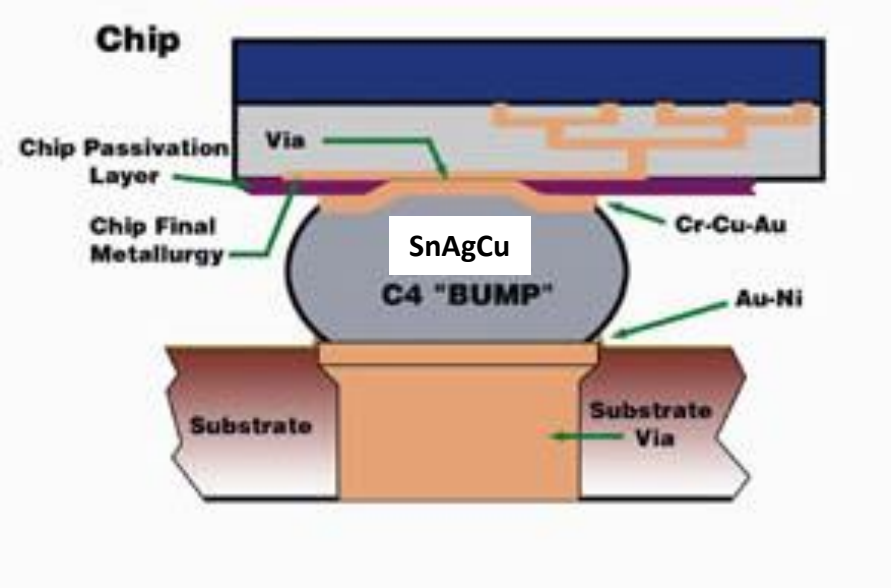


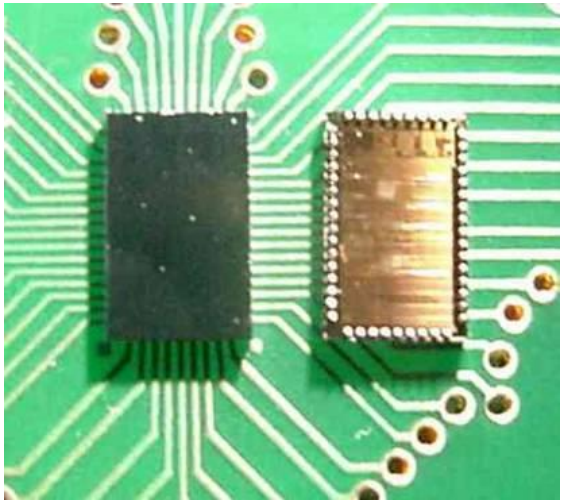
FR4 PCB, chip wirebonded to PCB, BGA (solder ball grid array) to attach to card.
Heat sink on the back

Example of an IBM chip (circa 2000)

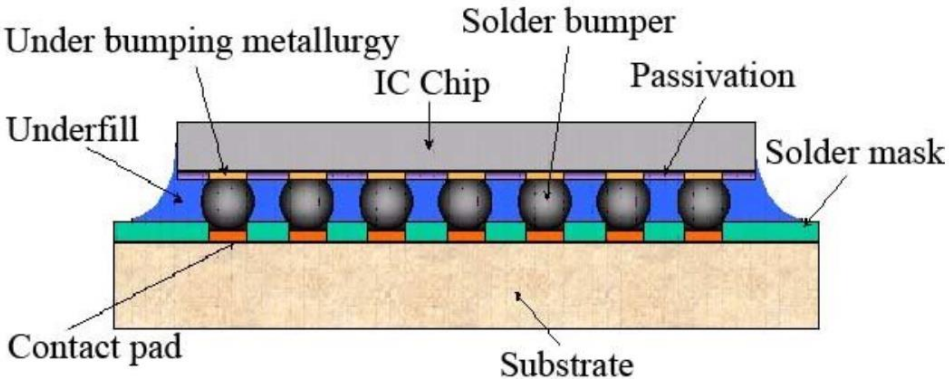


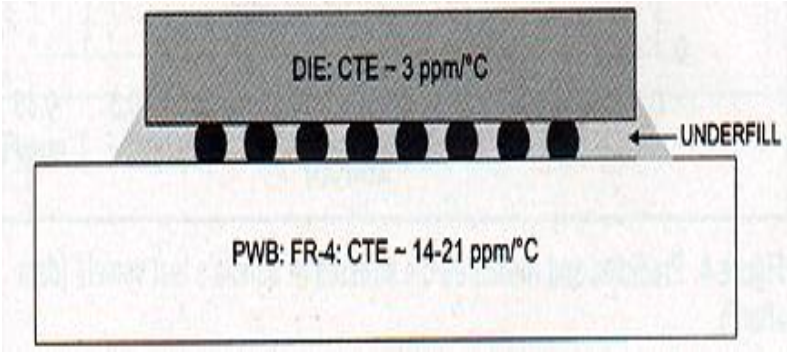
Flip-Chip





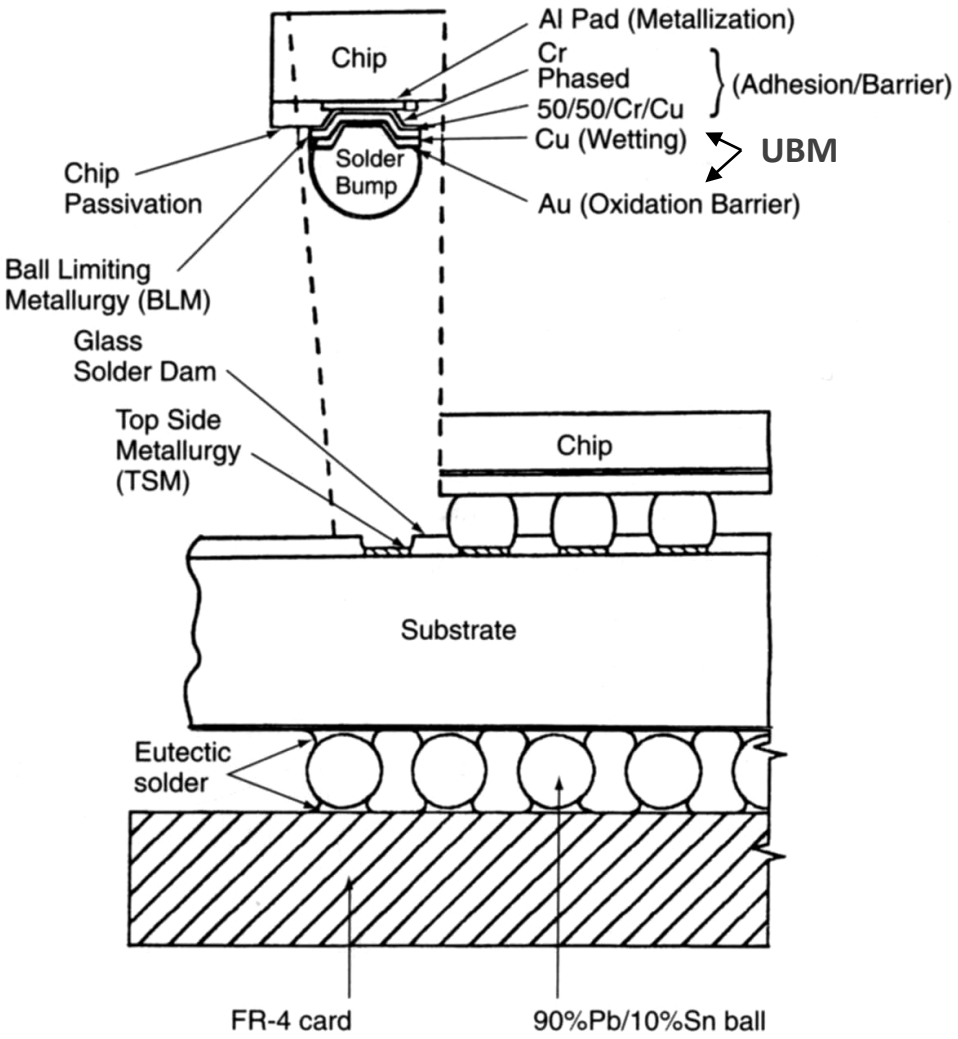
Then encapsulated with polymers: epoxy underfill in between chip and substrate + polymer (glob top) for top protection/fixation





Solder bump Flip Chip

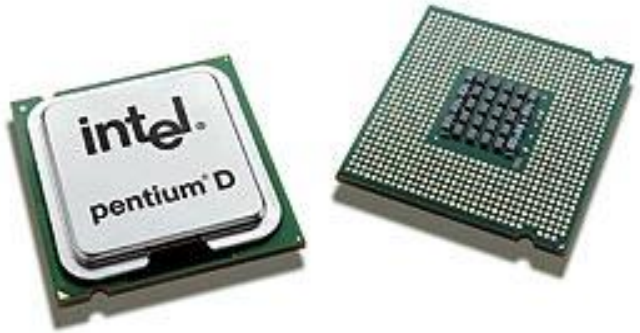
UBM: under bump metallisation required



Complex metallurgy (Al pad, Cr to hold Cu, with Au to protect) (can lead to corrosion problems if water is present)

Stress: expect shear stress to be larger the further from the center of the chip if chip and package not perfectly matched

Use underfill polymer to hold it all in place and relieve stress.

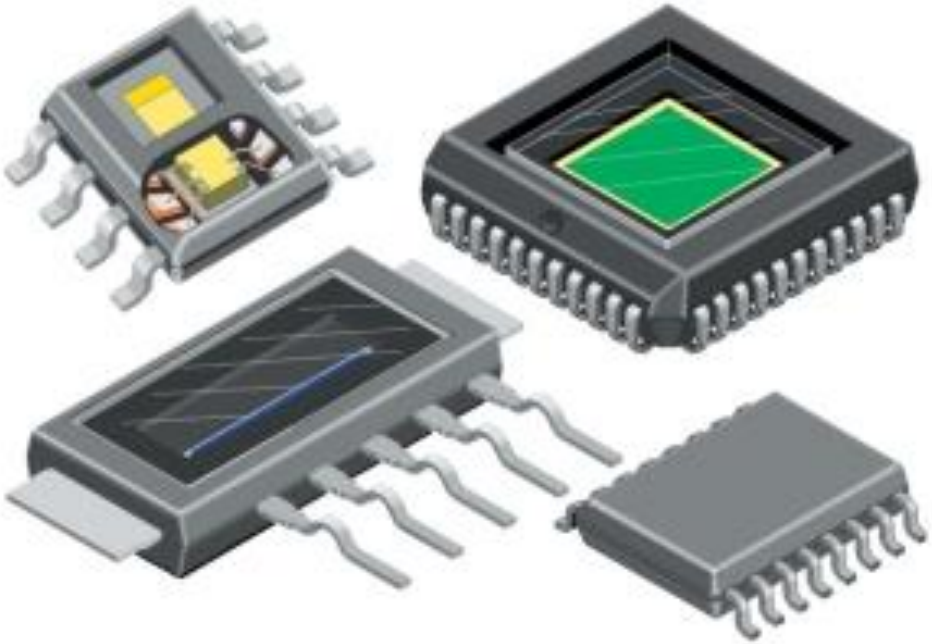


M. Ohring, p. 426

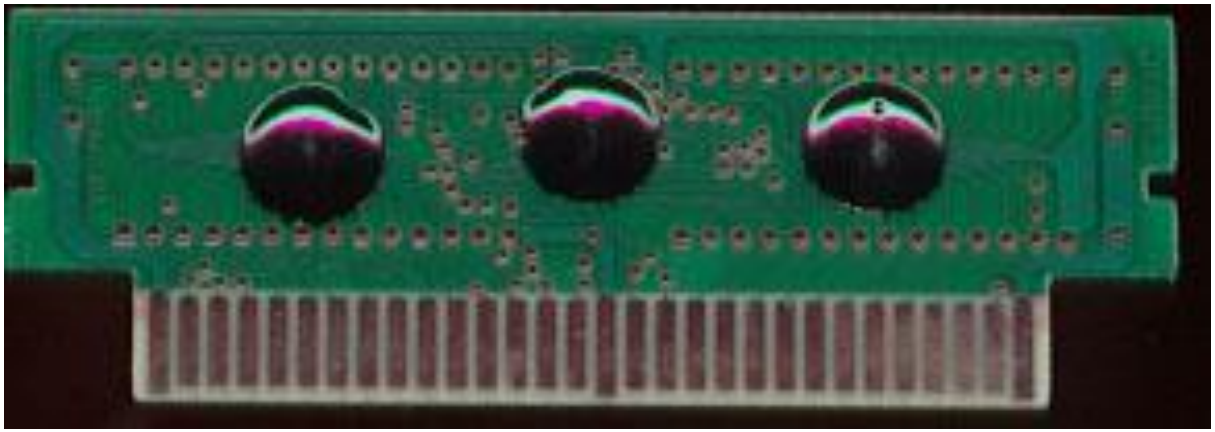
Surface mount package

- Gluing the chip in a surface mount package
- Wire bonding
- Soldering on the PCB

Surface mount devices (SMD)



Chip on Board (COB)



Super Donkey Kong cartridge (Nintendo)

3 chips: glued to PCB, wire bonded, Glob Top

- Very cheap solution!
- Short signal lengths
- Easy to change layout

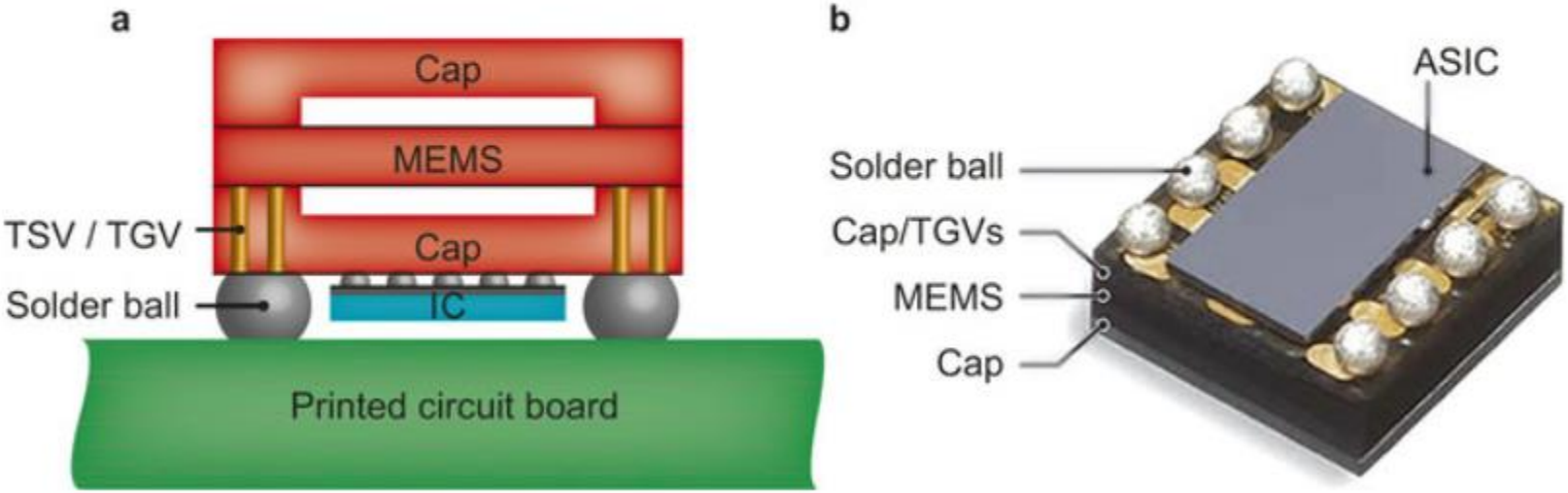
But:

- must handle bare die,
- not suited for high density or high performance (thermal, RF)

Chip scale packaging

Figure 4: Chip-scale package (CSP): the MEMS and IC chips are attached via face-to-face flip-chip bonding. (b) Photograph of a 3-axis accelerometer (VTI, CMA 3000) fabricated using chip-on-MEMS technology. Package dimensions: 2 × 2 × 1 mm3. From Ref 61.

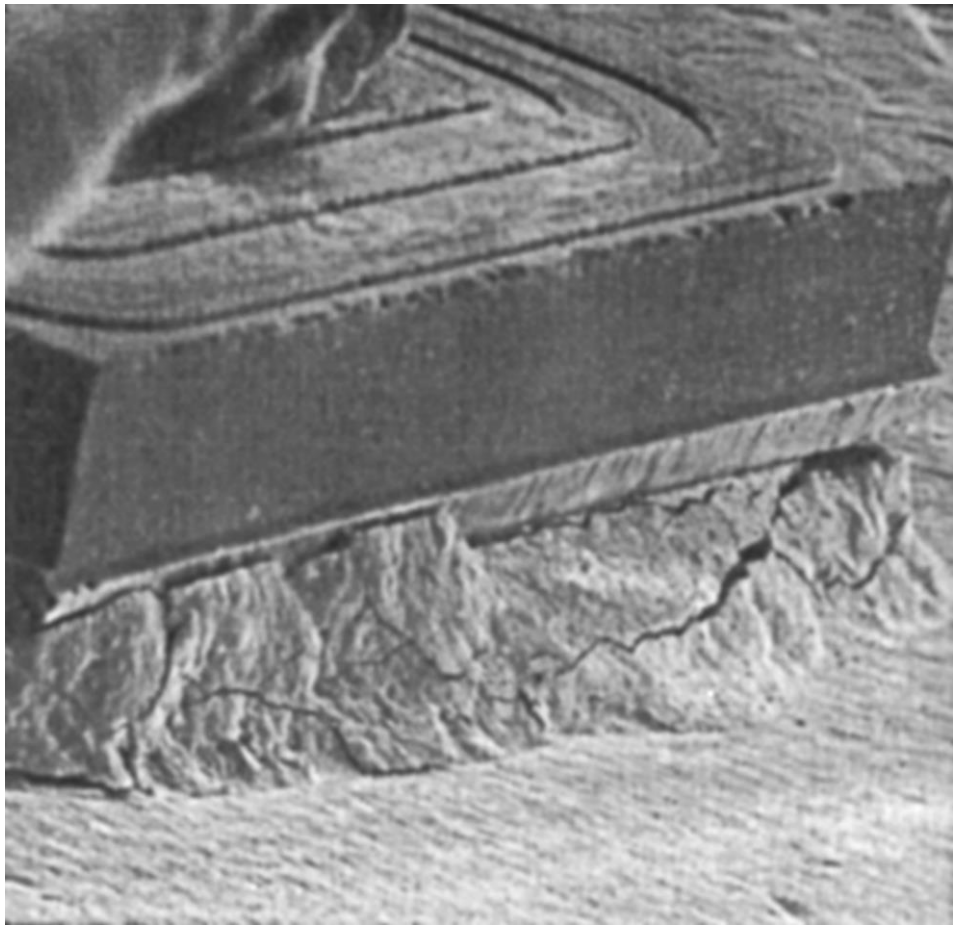
Integrating MEMS and IC, Microsystems and Nanoengineering 2015



• In order to qualify as chip scale, the package must have an area no greater than 1.2 times that of the die and it must be a single-die, direct surface mountable package.

• Another criterion that is often applied to qualify these packages as CSPs is their ball pitch should be not more than 1 mm.

Failure: Cracking due to CTE mismatch



From T.W. Lee, in *Microelectronic Failure Analysis,* ASM International, Materials Park, Ohio, USA, p. 344, 1993

$$\sigma = \frac{E_{chip}}{1-\nu}\left(\alpha_{chip} - \alpha_{substrate}\right)\left[T_{pack} - T_{op}\right]$$

Thermal stress given by above equation assuming zero stress at the packaging temperature T_{pack} and a perfect bonding of the chip.

Soft die-attach: risk deforming/cracking the die-attach

Hard die-attach: risk cracking the chip…

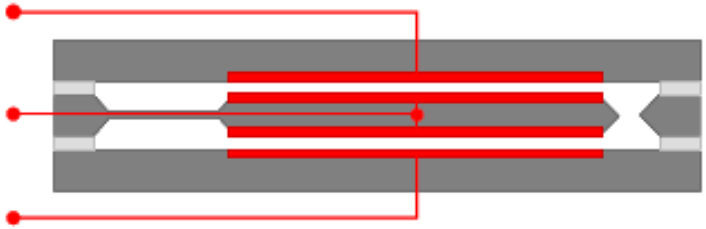
Summary: Microelectronic packaging components

- **Package: combination of different materials**
  - Metal
  - Ceramic & glass
  - Plastics / organics
- **Die attach:**
  - Glue chip to package with epoxy (cheap, fast, but outgasses and poor thermal conduction)
  - Solder chip to package (better thermal contact, higher temperature, must not melt with next thermal step).

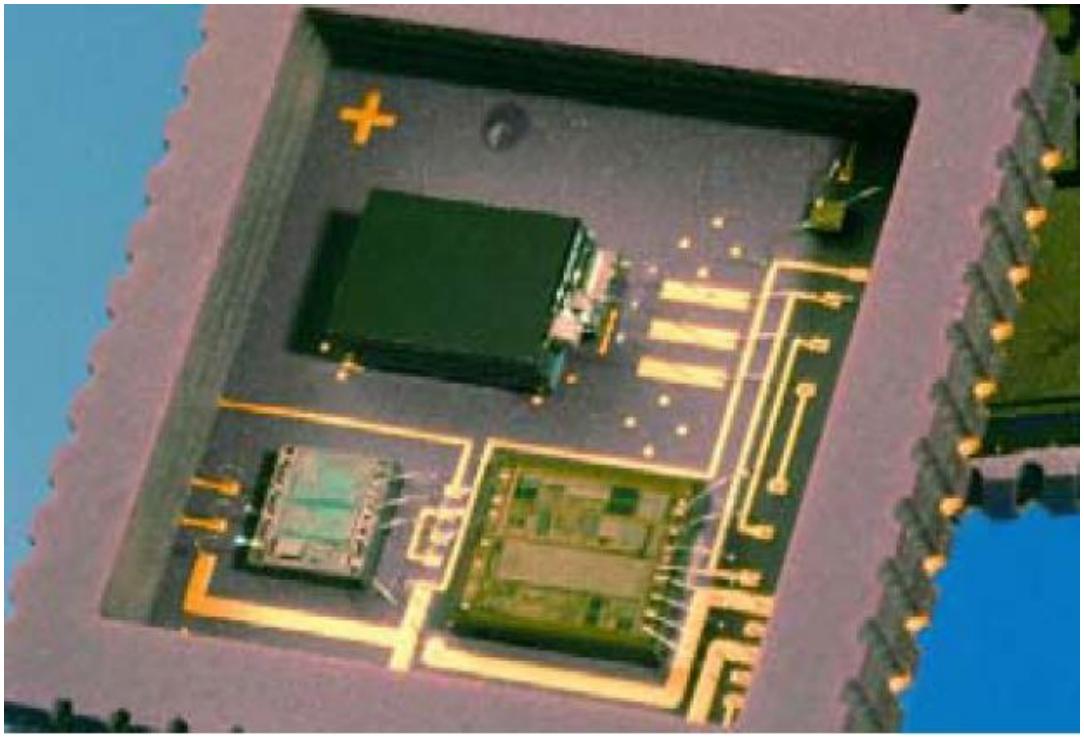
    Often eutectic Au-Si or 95%-5% Pb-Sn
    - Pb being phased out as WEEE (Waste Electrical and Electronic Equipment) European directive imposes the progressive suppression of lead in the electronic soldering from July 2006)
  - Glass frit: cheaper than metals, better CTE match, but low thermal conductivity
- **Electrical contact:**
  - Wire bond
  - Bump bond (Gold or solder bumps) / flip-chip

Specific packaging for Microsystems

Colibrys MS8000 accelerometer



Operates over a temperature range of –55°C to 125°C



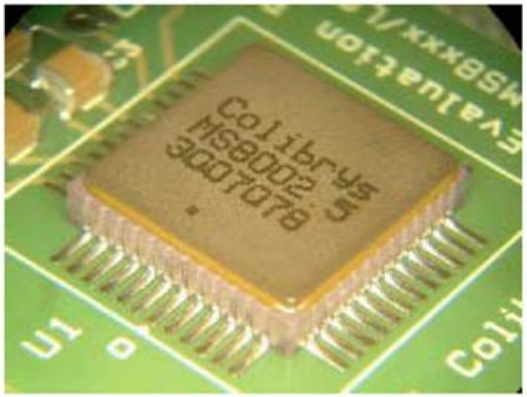
Accelerometer above made using silicon fusion bonding. Conductive electrodes for the capacitive operation made of doped silicon

4 chips in one package: electronics + accelerometer glued to package and wire bonded

Accelerometer chip very sensitive to stress (mechanical deformation) from die attach, fixation/connection process needs to be chosen carefully

Colibrys MS8000 accelerometer

- **Soldering of the packgaded MS8000**
  - **Recommend soldering all 48 pads (only 14 used electrically) for stress control**
  - **Standard bonding uses $Sn_{63}Pb_{37}$, but is phased out…**
  - **Main replacement is $Sn_{95.5}Ag_{3.8}Cu_{0.7}$**
  - **Other option: $Sn_{42}Bi_{58}$, 50% lower stress, lower temperature and CTE (under development)**

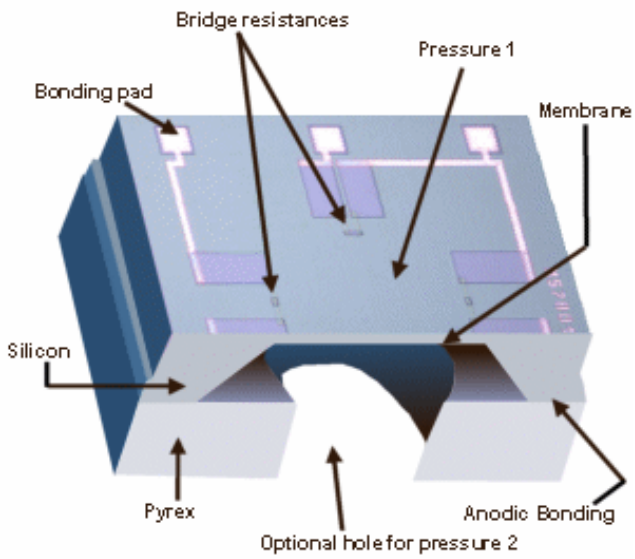


	Sn63Pb37	Sn95.5Ag3.8Cu0.7	Sn42Bi58
Melting point (°C)	183	216	138
CTE (ppm/°)	25	23	15
Tensile strength (MPa)	32	40	55

Intersema pressure sensor

- **Pressure sensors require access to the environment**

Absolute sensor requires a cavity hermetically sealed with a defined gas pressure as reference

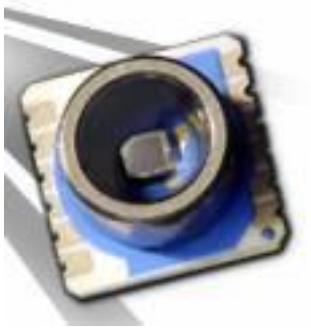


Differential pressure sensor

TE connectivity (Bevaix, CH)

Different packages allowing gas pressure to reach the sensor

Automotive



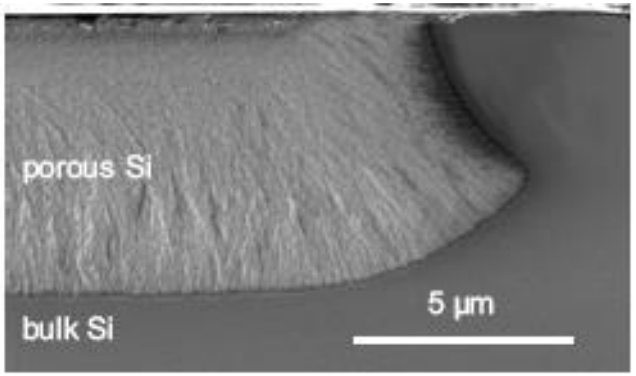
Barometric

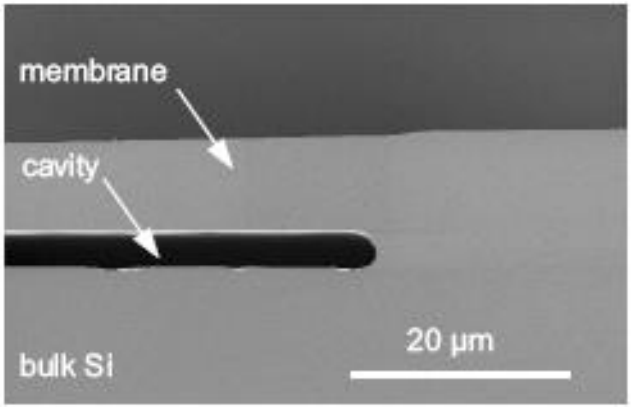
Environmental

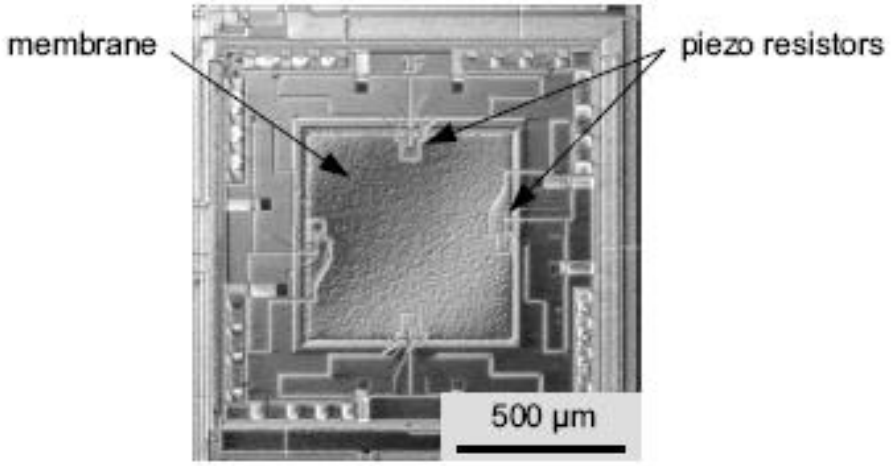
Bosch Sensortec
BME280

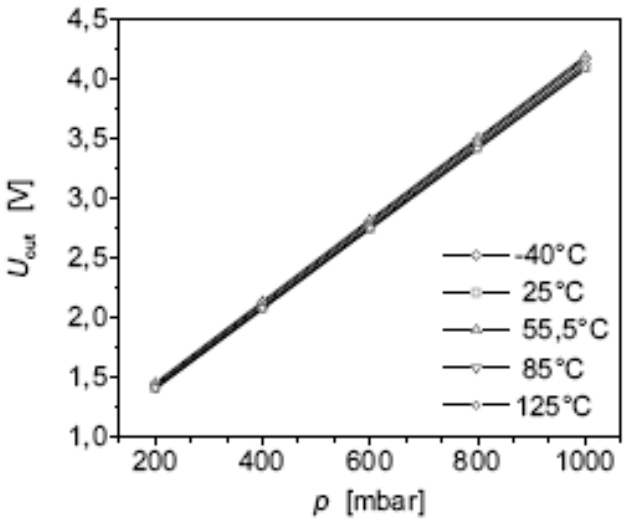
WLP Bosch pressure sensor

- Based on Porous Si to form the cavity
- Based on Epitaxial Si growth to form the membrane





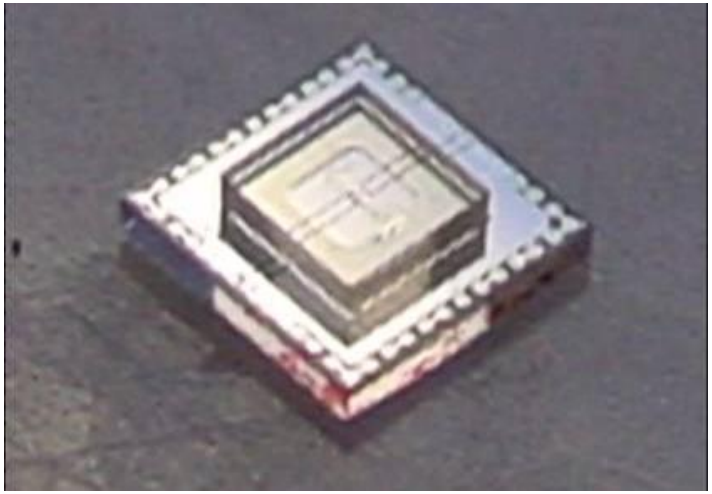




More information in Lesson on Sensors

Flip chip soldering process for Wafer level packaging

- **Wafer level packaging developed at IMEC**
  - **With IMEC's indent-reflow-sealing (IRS) method sealed cavities can be realized at wafer level. It provides both hermeticity of the cavity seal and controllability of the cavity ambient, two features essential for packaging MEMS.**
  - **The method is based on a two-chip approach whereby the chips are flip-chip assembled using a solder bond. An optional spacer layer is implemented underneath the solder layer of the first chip to allow a better control of the cavity height. Solder reflow and sealing is performed in a dedicated oven with pressure and gas control.**



Flip chip soldering process for Wafer level packaging

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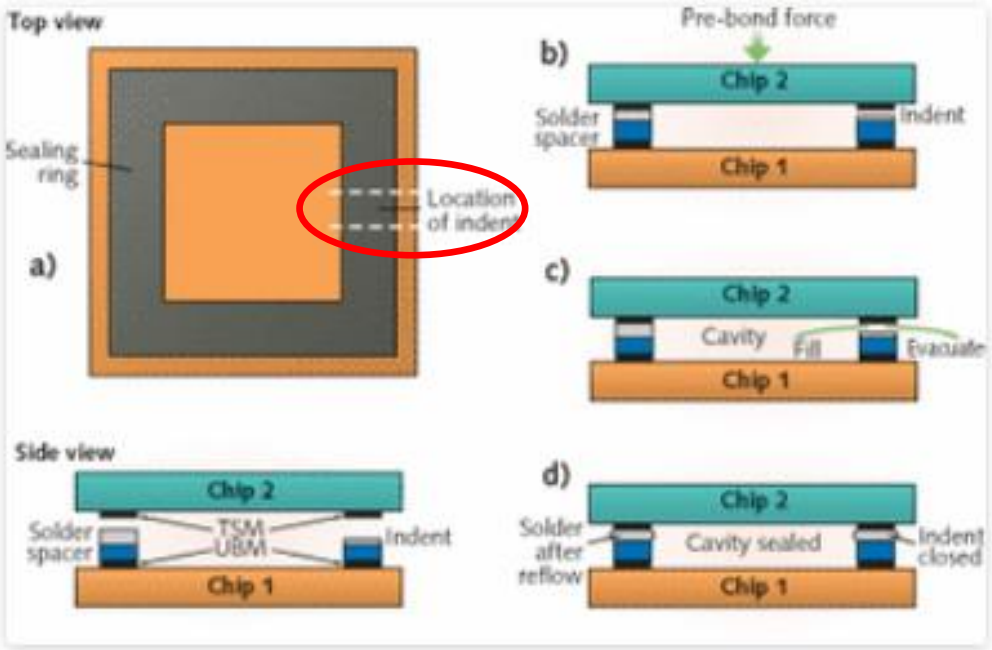
  - **IMEC's indent-reflow-sealing (IRS) method**

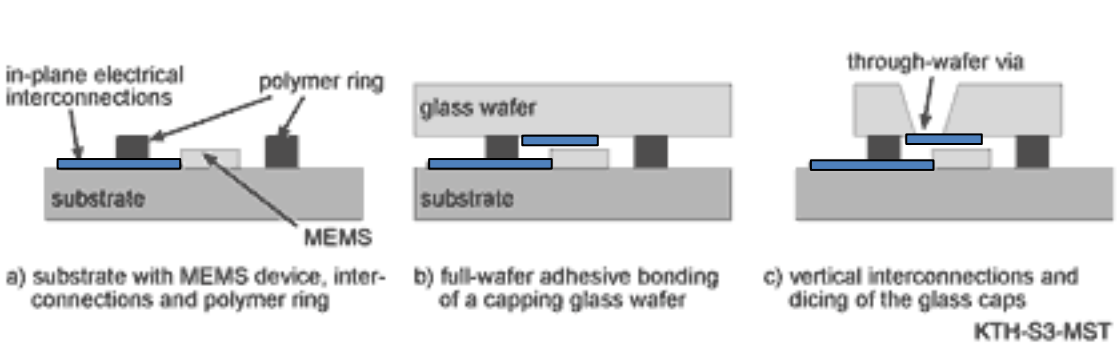


Insulating spacer used to define the height of the cavity. Also interconnection metallization can be routed out the cavity by passing below the spacer (solder on top)

Gap introduced between solder and chip during heating step to suck the flux (used for better wettability of solder on metal pad) gas coming out from the solder

Adhesive bonding for Wafer level packaging

- **Wafer-level packaging by using a patterned adhesive layer.**
- **A technique which allows the parallel packaging of all devices by one full-wafer bonding step. The separation of the capping lids is done afterwards by dicing, together with or separate from the substrate wafer. To electrically connect such packaged devices, thick film in-plane interconnections through the polymer sidewall where utilized as well as through wafer vias by using a novel two-step etch-technology, based on powder-blasted recesses in the back-side of the glass wafers.**



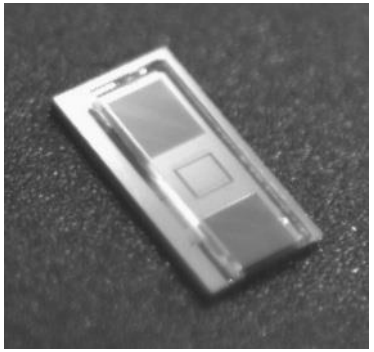


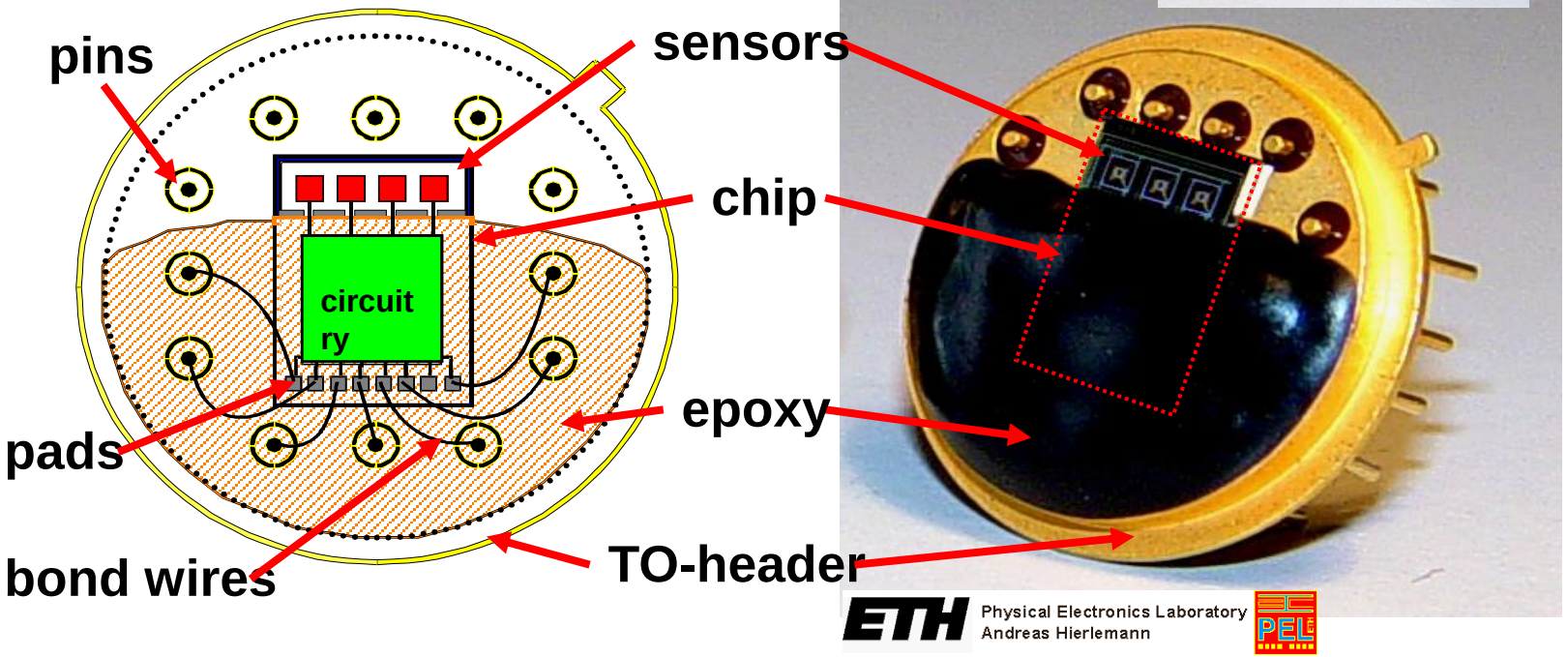
Figure 1. Rough overview of the fabrication procedure of wafer-level packaging by full wafer bonding with a patterned adhesive layer, including in-plane interconnections through the polymer wall and vertical interconnections through the capping glass wafer (in blue).

- **Benzocyclobutene (BCB) is the polymer mainly used for the bonding experiments. The recent efforts in patterned adhesive packaging of MEMS devices are to improve the bond strength of pre-cured polymer materials and gas tightness of the polymers by adding a cladding layer.**

From KTH, Sweden

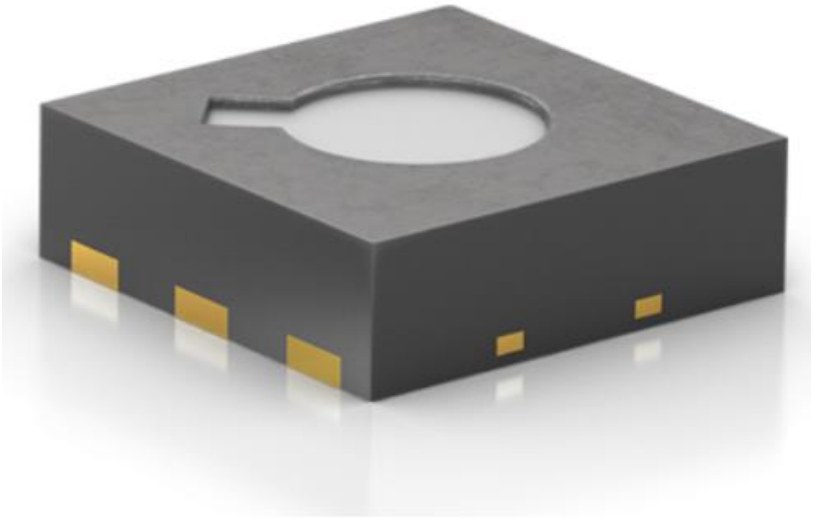
TO packages

- Wire bonding chip to TO
- Epoxy protection of the electronics
- Cap with gas permable membrane
- Cap fixed with glue on TO



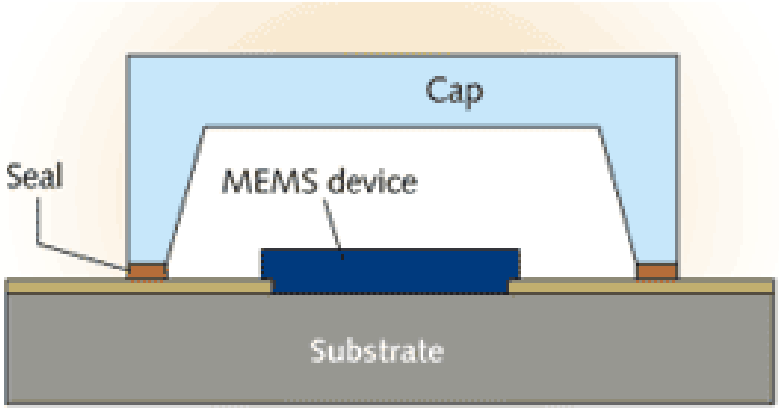
Packaging of chemical gas sensors

- **SMD based plastic molded packages**
  - **Array of metal-oxide gas sensors on silicon from Sensirion**
  - **Small 2.45 × 2.45 × 0.9 mm^3 DFN package featuring an I^2C interface**

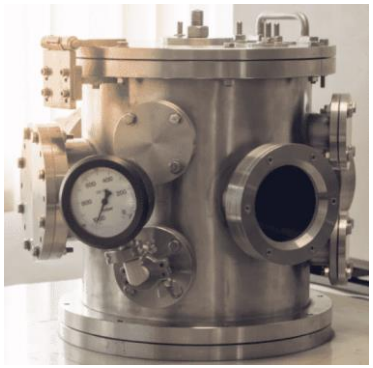


DFN - Dual Flat No Leads: DFN is a very small square-shaped or rectangular surface-mount plastic package with no leads. Metal pads or lands along two sides of the bottom of the *DFN package* serve as electrical connection points to the outside world.

Hermetic packaging



Challenges to seal MEMS micro-scale devices in comparison to large vacuum chambers ?



Hermetic capping of MEMS

- **Protection sensor structure**
  dust, humidity, mechanical handling during test, assembly, wire bonding

- **Mechanical stability of package**
  during handling, die bonding, thermo-mechanical stress during operation, mechanical load during field use

- **Defined vacuum**
  damping affects sensitivity, low power consumption, less temperature effects, compatible to getter activation

- **Long term stability**
  long term hermeticity, temperature cycle stress corrosion, 15 years operation in cars, 20 years in avionics

Vacuum requirements for MEMS

Sensor Type	Working pressure [mbar]
Accelerometer	~300-700
Absolute pressure sensor	~1-10
Resonator (angular rate)	10^{-1} - 10^{-4}
Gyroscope	10^{-1} - 10^{-4}
RF switch	10^{-1} - 10^{-4}
Microbolometer	> 10^{-4}
Optical MEMS	moisture free
DMD-DLP	moisture free

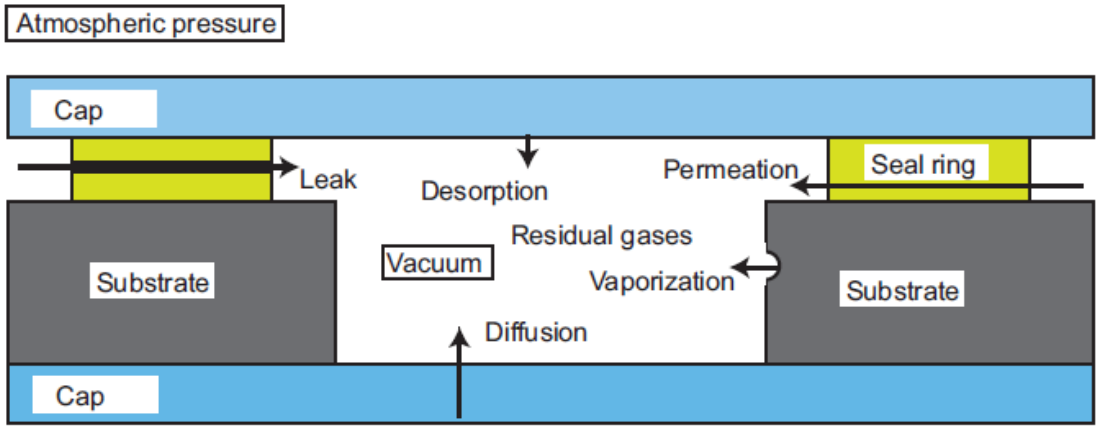
Atmospheric pressure :1.01325 bar

Gas sources in MEMS devices

The main contamination sources that cause degradation in MEMS can be divided in two categories:

1. **Vapor and gas flux** during the lifetime
   - gas which penetrates into the system as a result of leakage
   - gas coming from the outgassing of materials present in the system
   - gas entering the system by permeation through walls, windows, etc.

2. **Residual gases**: gas molecules of the initial atmosphere enclosed in the system, just after the sealing or outgassed during the process



Basics of getters

- A getter is an efficient “small” chemical pump which is able to sorb the gaseous impurities by fixing them as stable chemical compounds

- A getter is characterized by
  - Capacity
  - Speed
  - Selectivity
  - Condition of use (activation and sorption temperature)

	With Getter	Without Getter
Pressure after bonding (mbar)	$<< 10^{-4}$	1
Pressure after 5 years (mbar)	$<< 10^{-4}$	2.7

Role and requirements of a getter

Role of a Getter	Requirements for a Getter
■ Removal of gases ■ Maintenance of vacuum ■ Sorption of gas bursts ■ Minipump during processing	■ Chemical stability ■ Mechanical stability ■ Absence of particles ■ Low gas emission ■ Easy and uniform activation ■ Easy and safe handling

Families of getters

Coatings or Pellets

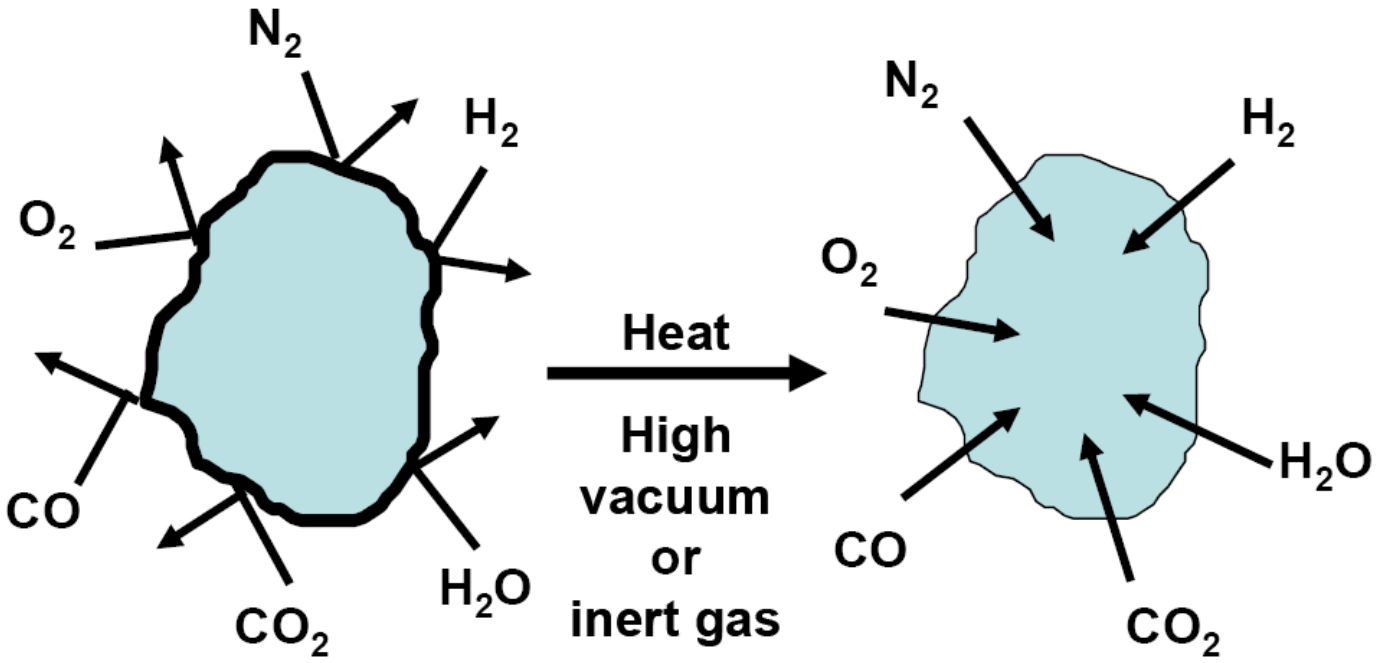
Evaporable	Non-evaporable (NEG)
Ca, Sr, Ba, Ti*	Ti*, Zr, Th

Key characteristic: **Surface** **Porosity**

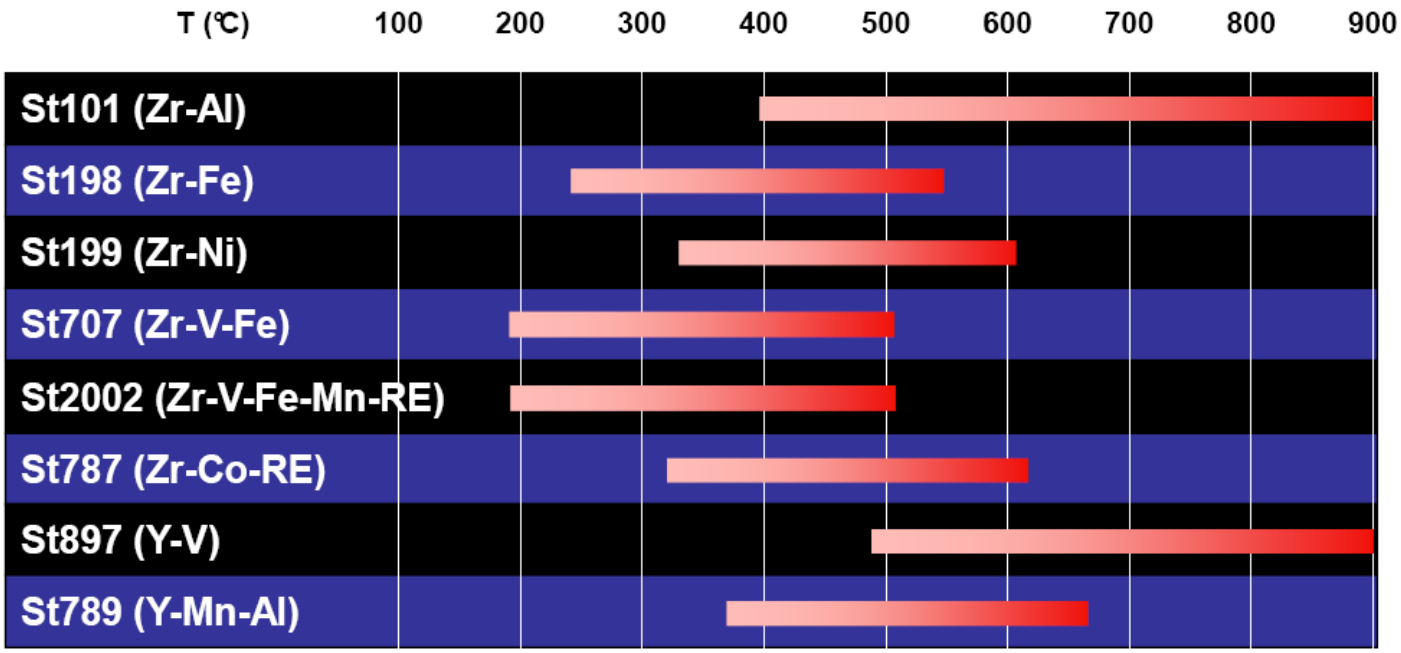
- Ti can act as both an evaporable (meaning coating by a flash of material) and a non-evaporable getter (solid film /pellet)

NEG activation

(= passivation layer removal)

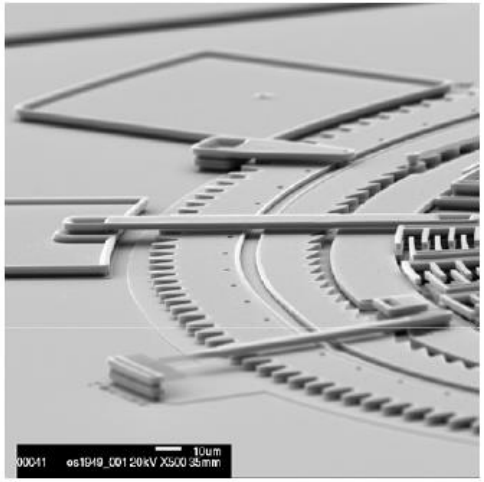


NEG examples

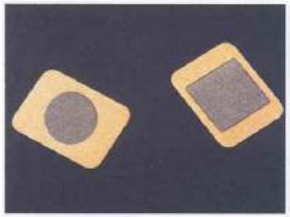


Ideally getter thermal activation is performed during the bonding process of the hermectic cap
(post laser activation through a glass cap possible)

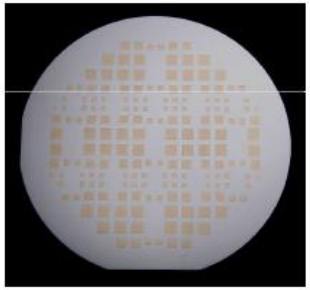
Examples of getters from SAES



MEMS that require vacuum or inert gas



PageLid™ for discrete packaging



PageWafer™ for wafer level packaging

- PageLid for single device encapsulation
- PageWafer for multiple devices encapsulation

Vacuum packaging: Comparison and leak rate

	Anodic bonding	Fusion bond-ing	Surface activated bonding	Glass frit bonding	Eutectic bonding	Soldering
Bonding Temperature [°C]	200-500	>800	200-400	430	AuSi: 400 AuSn: 300 AlSi: 600	>120
Bond strength	T>300: high	high	medium	low	high	high
Outgassing during bonding	O_2	H_2, H_2O	H_2O	CO, CxHy	very low	H_2O
Tolerance to topography	almost 0	0	0	large	1.5 µm	large
Leak rate	low	very low	n.a.	low	very low	very low

The leak rate *L*, the evolution of the pressure *P* inside a cell is proportional to the difference of internal and external pressures and can be expressed by:

$$\frac{dP}{dt} = \frac{L}{P_{norm} V_0}(P_{ext} - P)$$

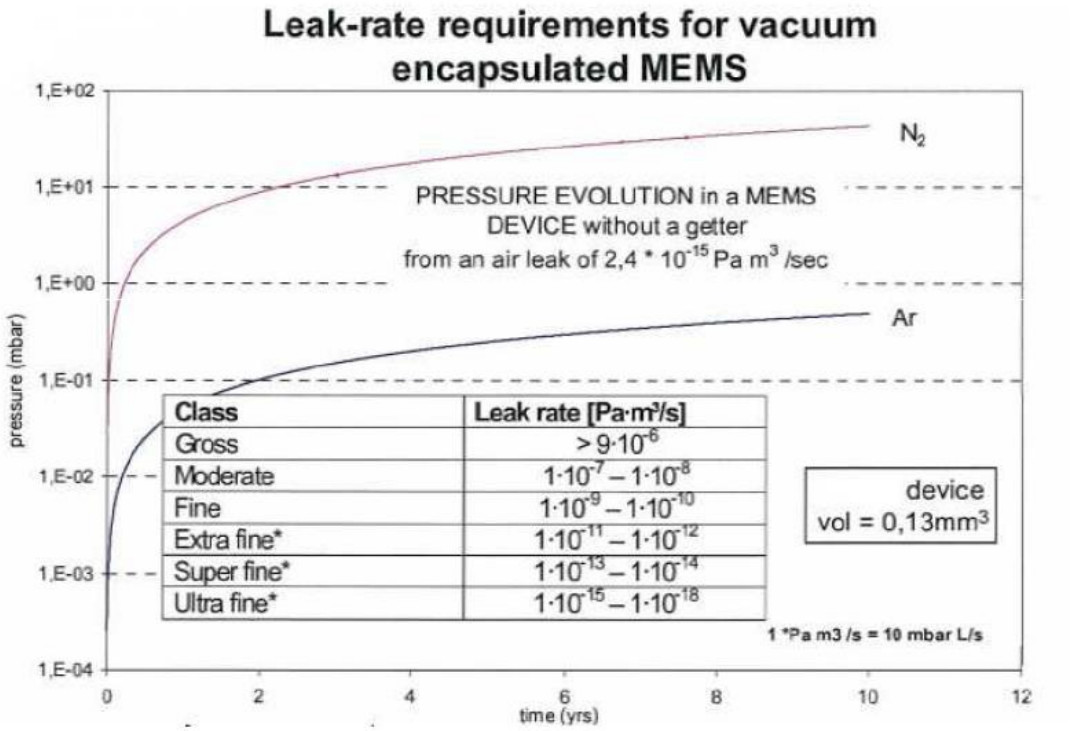
V_0 is the volume of the cell cavity,
Pnorm a normalization pressure of 1000 mbar
Pext the external pressure at which the sample is kept ,1013 mbar if at 1 atm.
P_0 *the initial pressure inside the cell at t = 0*

The pressure evolution is then: $P(t) = P_{ext} - (P_{ext} - P_0) \cdot e^{-(Lt)/(V_0 P_{norm})}$

If the pressure variations are small compared to the external pressure, a linear approximation can be made for *L:*

$$L = V\frac{\Delta P}{\Delta t} \quad (\text{Pa}\bullet\text{m}^3/\text{s})$$

Leakage



Creating, maintaining and measuring a high vacuum or a stringently controlled atmosphere in nL-scale cavities poses challenges unique to wafer level cavity packaging.

The hermeticity test of MIL-883E, Method 1014.9 is invalid for cavity volumes under 1'000 nL

The low-nL cavity volumes typical of advanced devices requires new methods for determining hermeticity.

Even for a low leakage rate *L*, a fast pressure increase is expected in the first year as the pressure difference that drives the leakage is large and the cavity volume very small.

Due to the exponential nature of the relation, the pressure increase slows down with a higher pressure inside the package.

Techniques to measure hermeticity in MEMS packaging

Describe the implementation of the following techniques used to measure the quality of the hermicity of MEMS packaging

1. Membrane deflection
2. Resonator
3. IR spectroscopy

For each technique give information on:

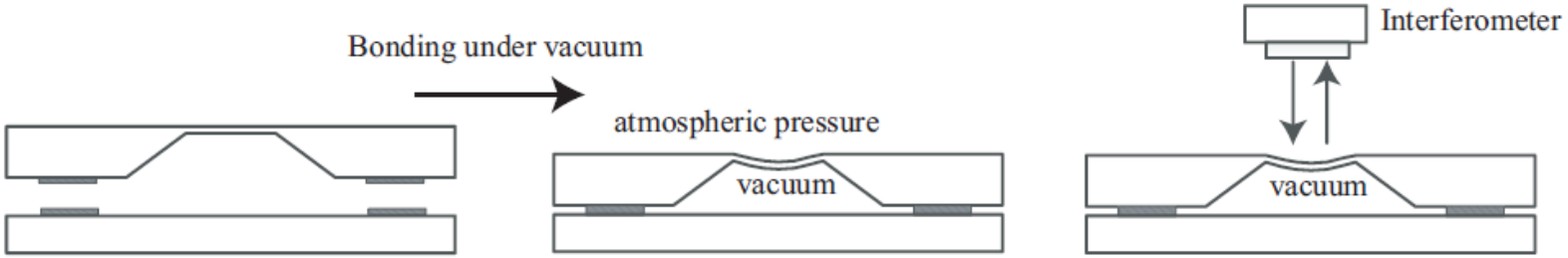
- Structure design and materials
- How the variation of pressure is measured experimentally

Method 1

Measurement of sealing hermeticity (leakage rate) using

Membrane deflection method

- Monitoring of the membrane deflection over time
- Precision on leak rate is limited due to unprecision in the physical properties of the materials and for some experimental parameters (dimensions)



If the deflections are small compared to the size of the membrane, they can be analytically related to the pressure difference* using:

$$P_D = C_1 \frac{t d^3}{a^4} \frac{E}{(1-\nu)} + C_2 \frac{t^3 d}{a^4} \frac{E}{(1-\nu^2)}$$

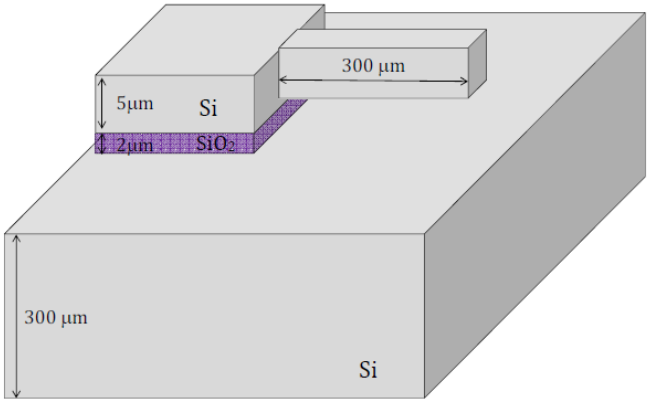
E is the Young's modulus and ν the Poisson ratio
t the thickness of the membrane
d the maximal deflection
a half the length of the square membrane.
$C1$ and $C2$ are coefficients depending on the shape and material of the membrane, for square membrane $C1 = 1.84$ and $C2 = 4.129$

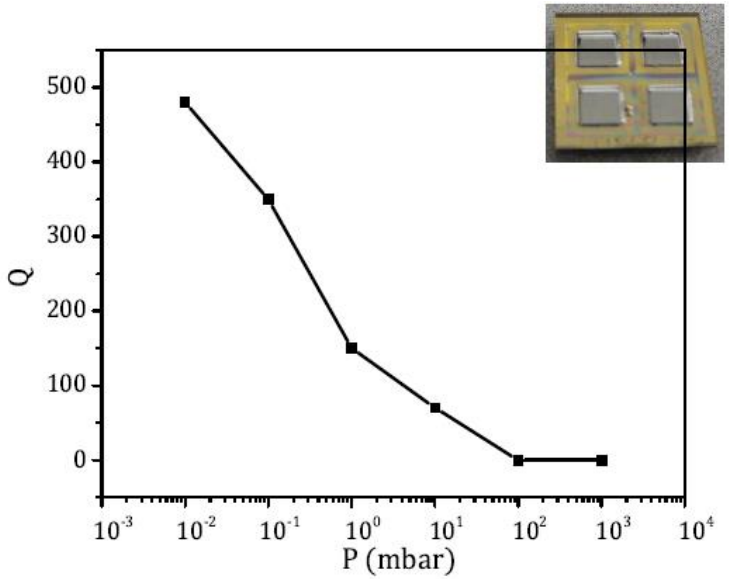
*assuming zero residual stress in the membrane

Method 2

Measurement of sealing hermeticity (leakage rate) using Resonator method

- Monitoring the Q factor of a encapsulated beam over time
- Use of piezoelectric mechanical actuation
- Use of Laser Doppler Vibrometry (LVD) to measure the beam displacement (transparent cap is needed)

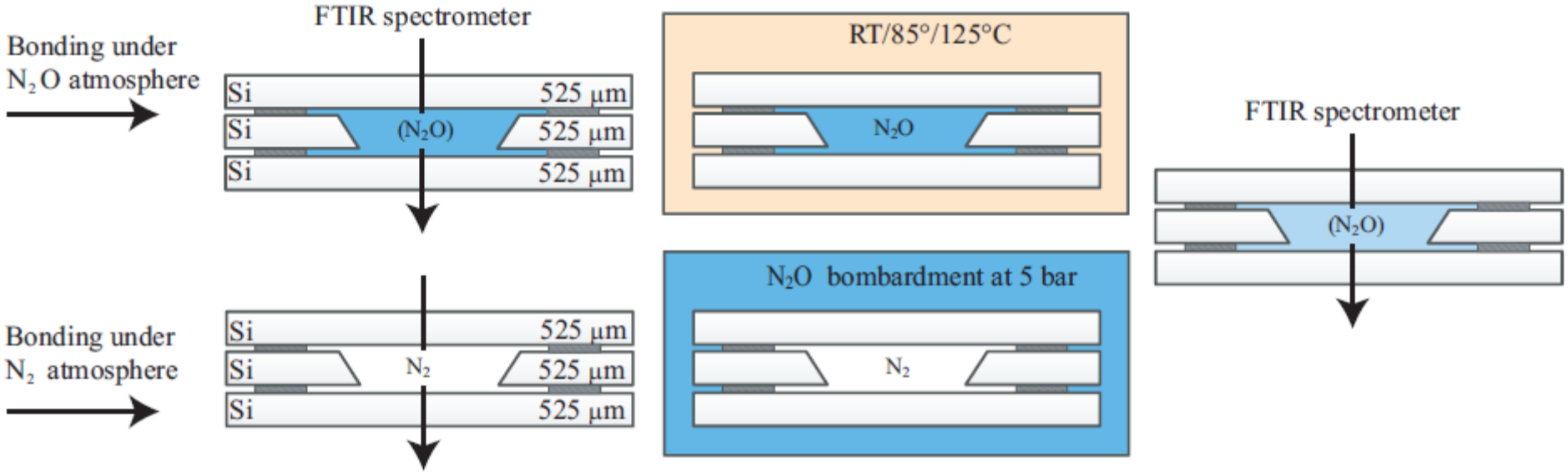




Calibration curve

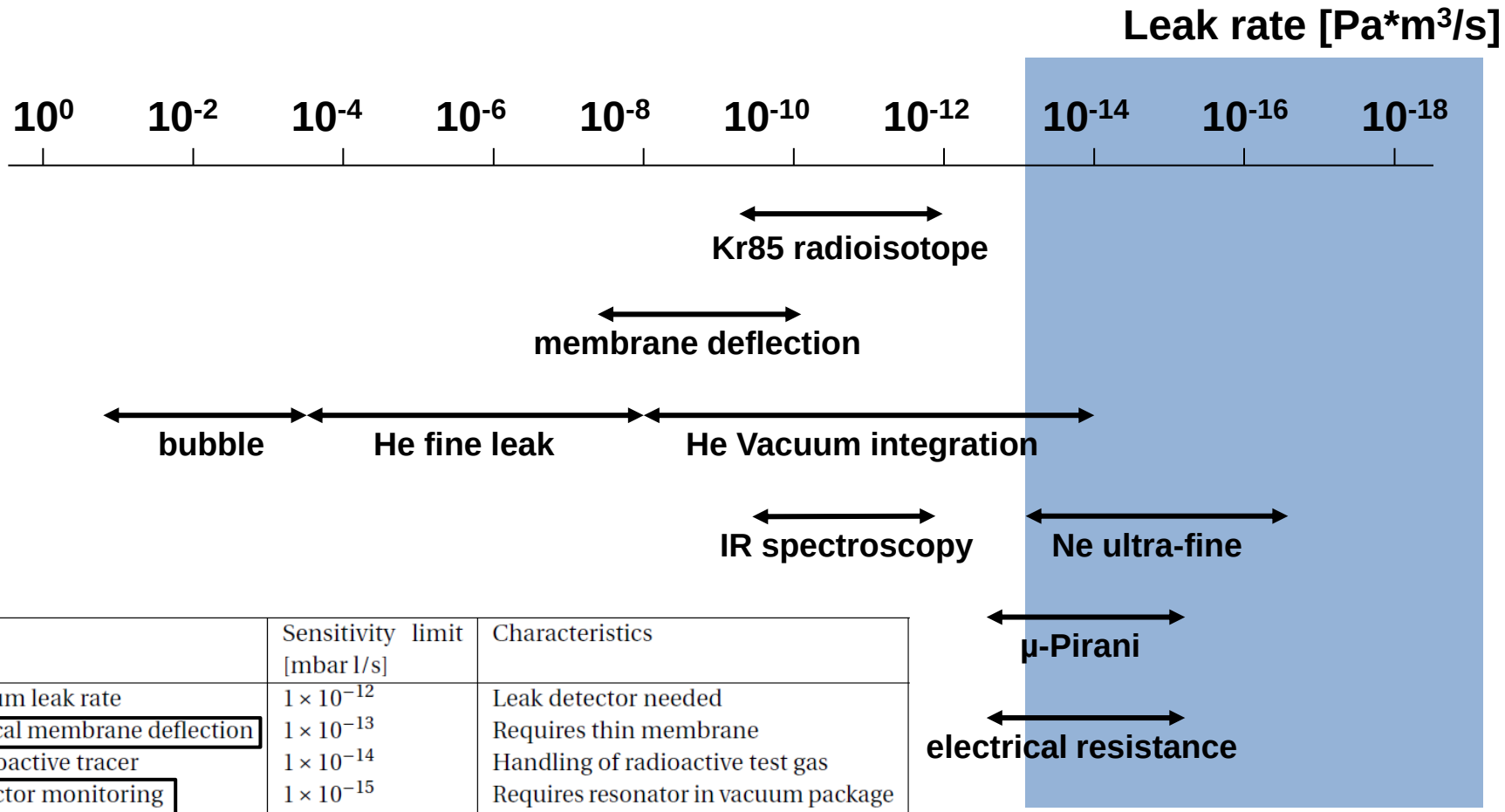
Method 3

Measurement of sealing hermeticity (leakage rate) using IR spectroscopy method



The absorption peaks N_2O are located at 2210 and 2240cm^{-1}, well below the absorption peak of CO_2 (around 2400 cm^{-1})

Hermeticity characterization



Test	Sensitivity limit [mbar l/s]	Characteristics
Helium leak rate	1×10^{-12}	Leak detector needed
Optical membrane deflection	1×10^{-13}	Requires thin membrane
Radioactive tracer	1×10^{-14}	Handling of radioactive test gas
Q-factor monitoring	1×10^{-15}	Requires resonator in vacuum package
Internal pressure	1×10^{-16}	Requires μ-Pirani pressure sensor
IR transmission	1×10^{-16}	Transmission of oxidized metal layer
Residual gas analysis	gas composition	Destructive test, for small packages

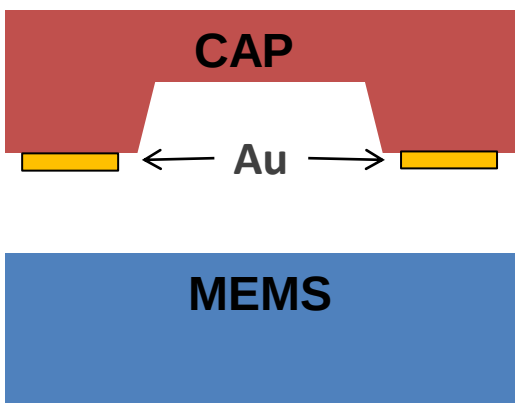
Leak rate measurement methods

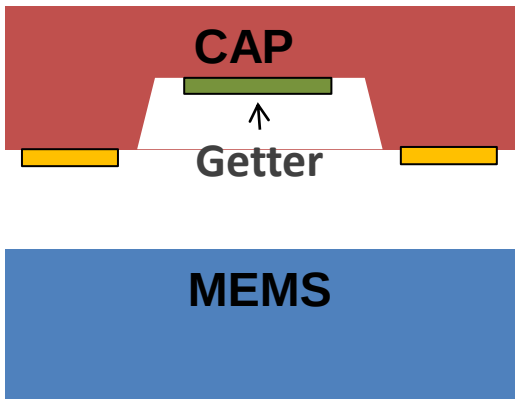
Test	Sensitivity limit [Pa.m^3/s]	Characteristics
Gross leak test	1*10^{-5}	Localization of gross leaks, verification of fine leaks detected by He/Kr55 leak test
Dye penetration	-	Inspection of weld seams material flaws
Pressure drop	1*10^{-6}	Inspection of pressure tanks and gas installations
Membrane resonance	1*10^{-9}	Requires thin (~20um) membrane, may affect sensor structures
Optical deformation	1*10^{-9}	Inspection of metal housings sensitivity affected by cap geometry
Helium leak test	1*10^{-13}	Limited to sealed volumes > 5mm^3
Radioactive tracer	1*10^{-15}	Handling of radioactive test gas
Q-factor monitoring	1*10^{-16}	Requires resonator in vacuum package
Internal pressure	1*10^{-16}	Requires micro-Pirani pressure sensor
IR transmission	1*10^{-17}	IR absorption of reference gas in cavity. IR transparency of materials. No getter integration.
Residual gas analysis	gas composition	Destructive test, laborious for small packages

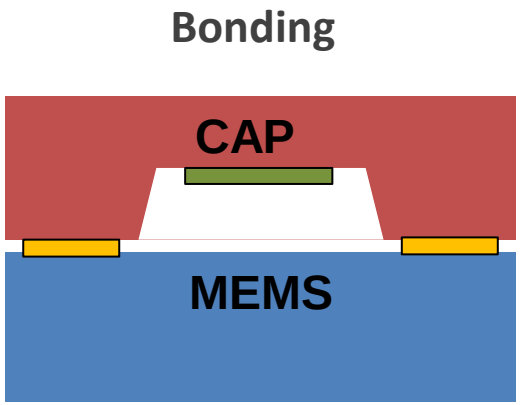
In blue suitable for MEMS vacuum level monitoring

Hermetic packaging: Typical process

- MEMS silicon wafer and glass Cap wafer
- Deposition of Au thin film bonding layer for eutectic bonding on Cap wafer
- Deposition of thin film getter layer in cap wafer
- Pump down the bonding chamber
- Apply pressure and temperature (400°C) for Au-Si eutectic bonding
- Getter film is activated during bonding process (post-laser activation possible)

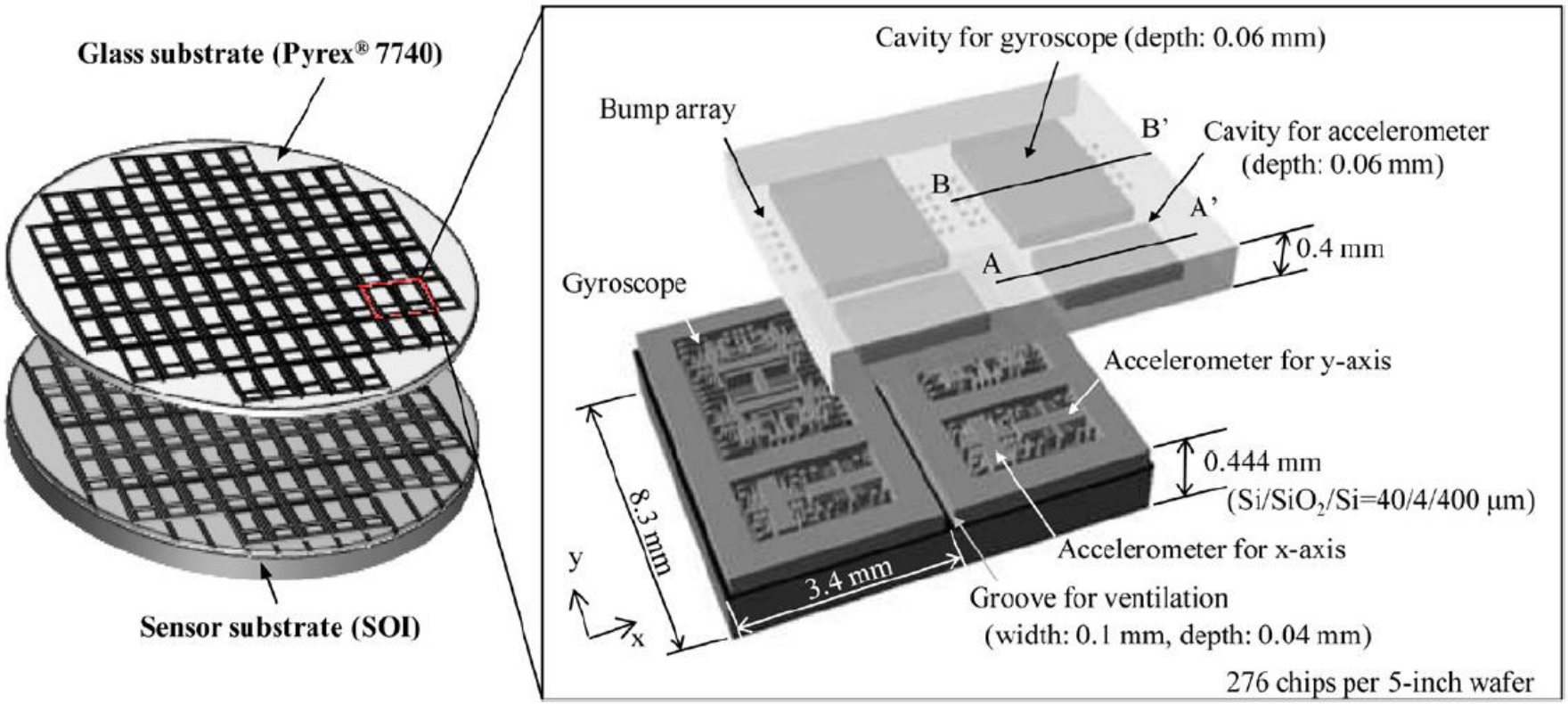






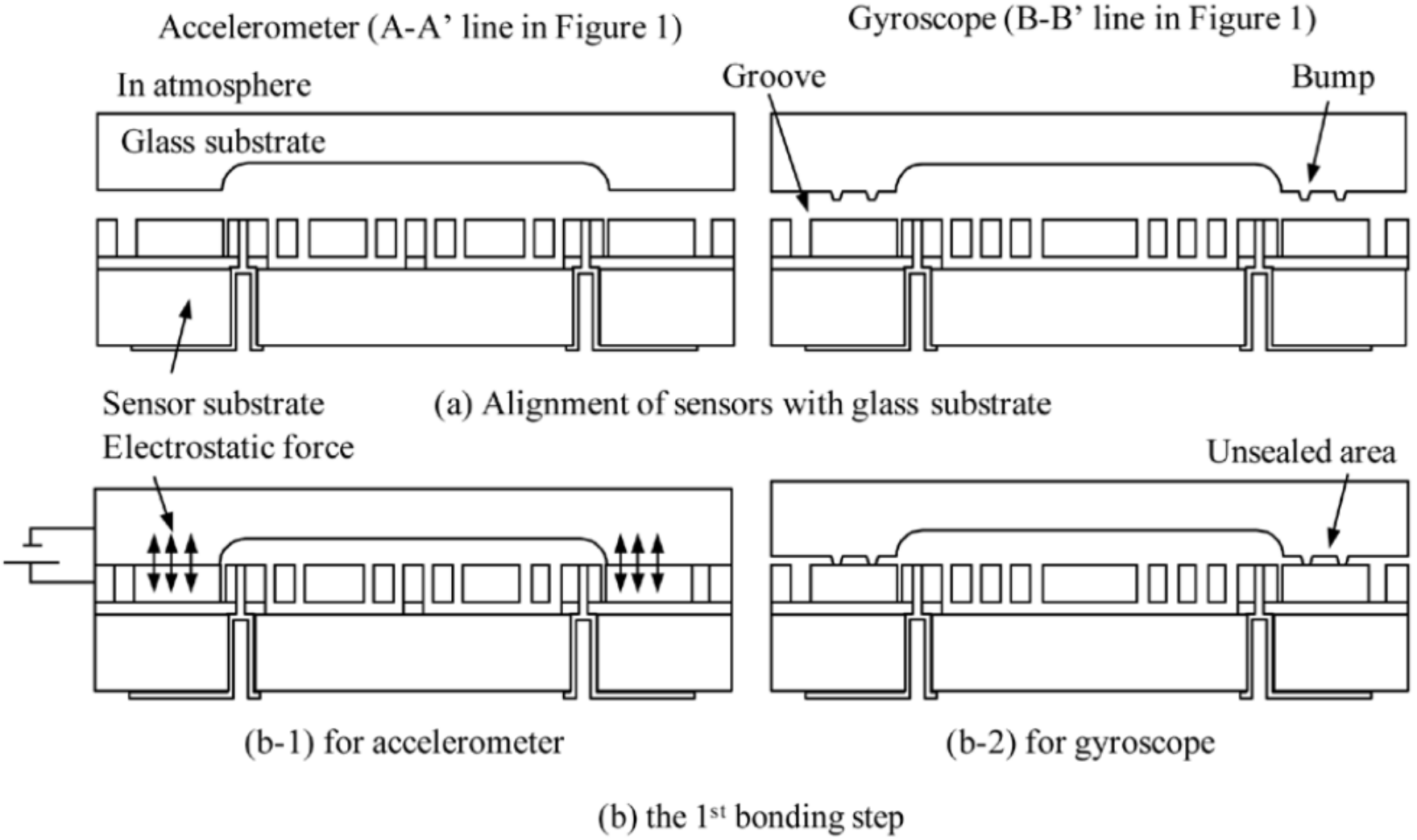
Hermetic packaging: Accelerometer + gyroscope

- Two-stage anodic bonding-based WLP between silicon and glass substrates for the simultaneous sealing of an accelerometer in the atmosphere and a gyroscope in a vacuum.

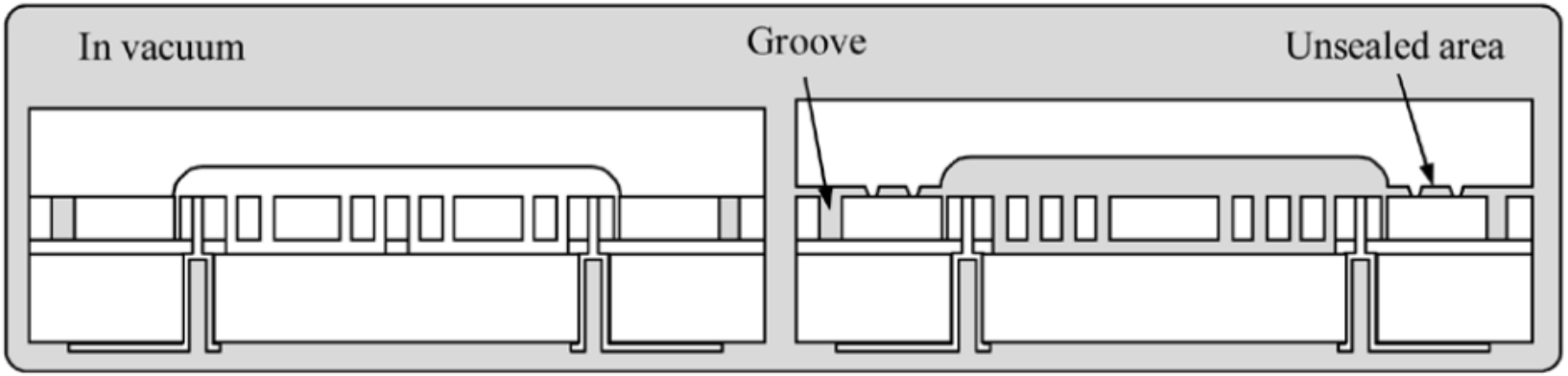


T. Aono *et al*., J. Micromech. Microeng. **26** (2016) 105007

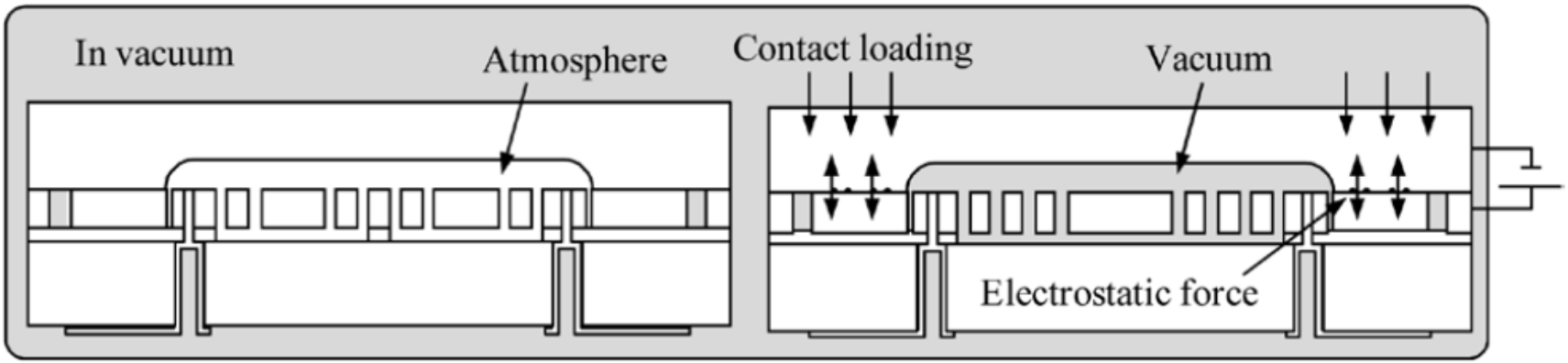
Hermetic packaging: Accelerometer + gyroscope



Hermetic packaging: Accelerometer + gyroscope



(c) Pressure control step



(d-1) for accelerometer (d-2) for gyroscope

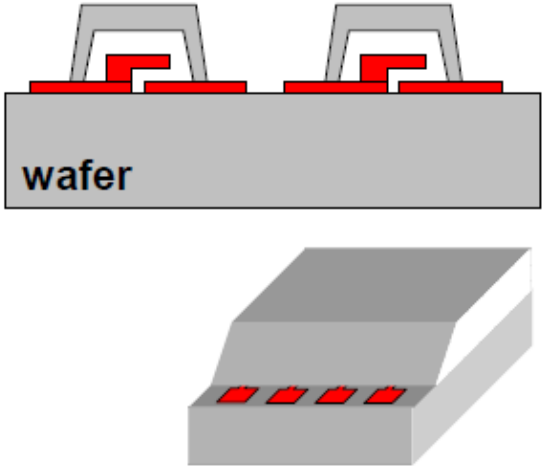
(d) the 2nd bonding step

Hermetic packaging: Accelerometer + gyroscope

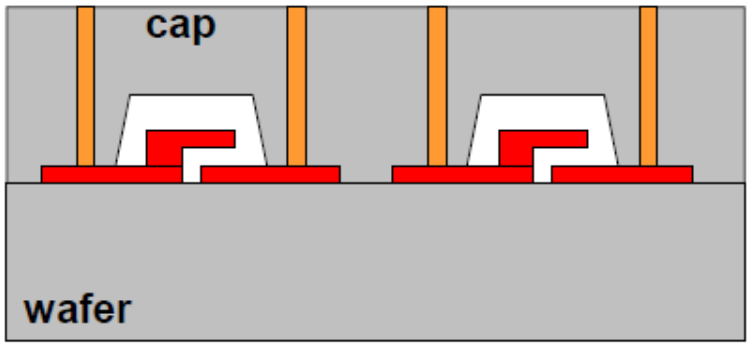
- **The key technique of this new WLP process is to prepare tiny bumps on the glass substrate which are regarded as surface roughness.**
- **The bumps can partially make unsealed areas between silicon and glass substrates so that sealed and unsealed areas are selectively formed at the interface**
- **The first bonding step is done to seal the accelerometer in the atmosphere**
  - The first anodic bonding step was performed at about 220-300°C with the applied voltage of 400 V for 30 min.
- **The second bonding step is done to seal the gyroscope at a high temperature under a high contact load in a vacuum**
  - The second bonding step was performed at about 500°C to soften the glass with load of 1 to 1.5 MPa at an atmospheric pressure of 0.1 Pa. The applied voltage of the anodic bonding was 400 V, and the bonding time was 30 min. Decreased temperature rate of -4°C/min for thermal-mechanical stress minimization

Electrical feedthroughs for device's connections

- Lateral surface feedthroughs
  - \+ Simplest fabrication
  - – Larger on-chip area required
  - – Not a true chip scale package (substrate required)
  - – Wire bonding required



- Through-silicon vias
  - \+ Small area required
  - \+ True chip scale package (BGA-ready) : solder bumps on top of vias
  - – Expensive processing



Lateral surface feedthroughs

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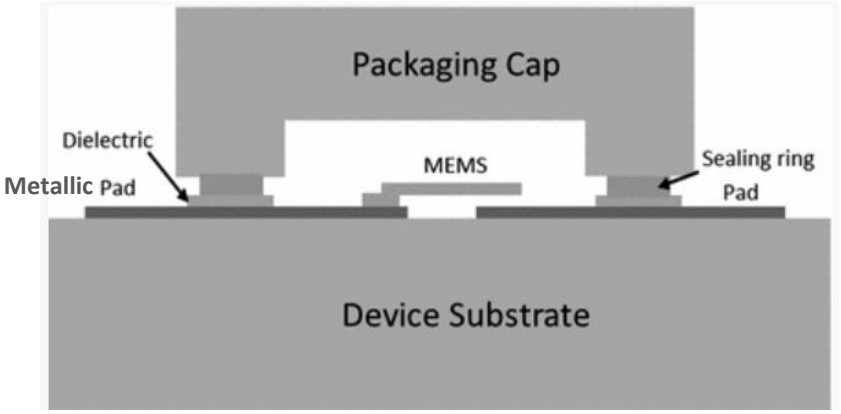
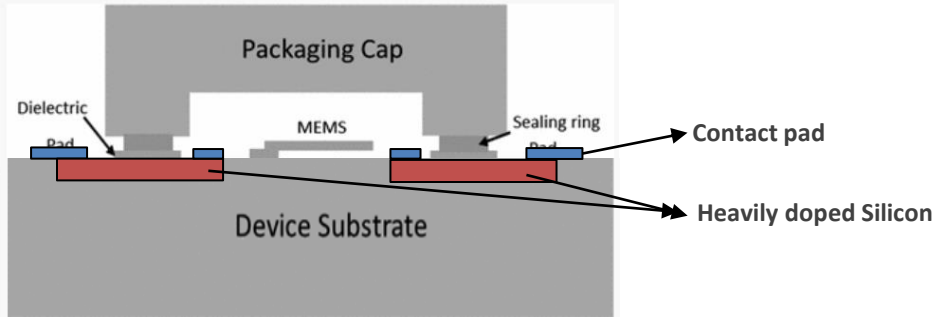
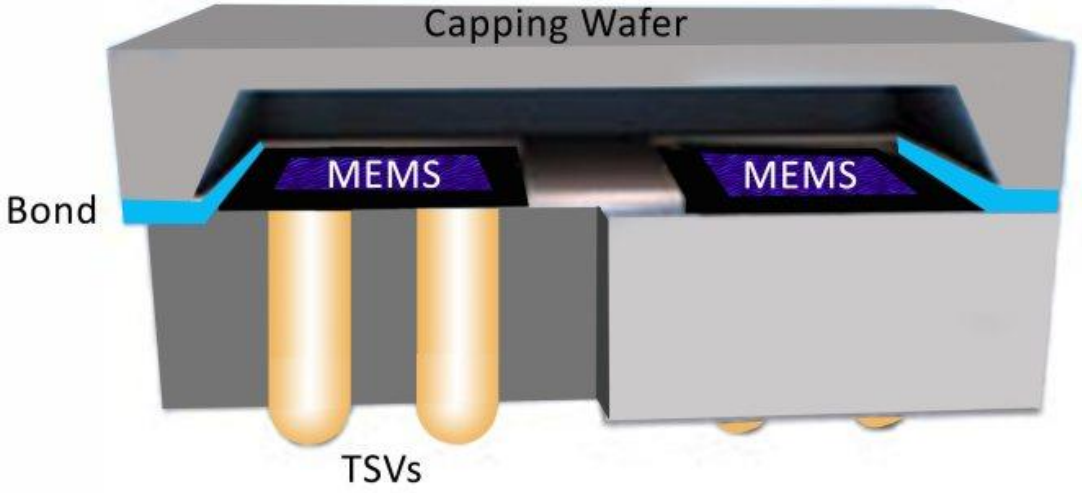


When bonding the cap wafer: the main issue is to avoid short cuts and to cover the step of the metallization

- Use of glass cap and non conductive bonding layer
- Passivation of the metallic interconnect (i.e. Al) with a thin dielectric film (silicon nitride or oxide), leading to steps to cover during the bonding process
- Embedded the interconnection by doping the silicon wafer underneath the bonding area

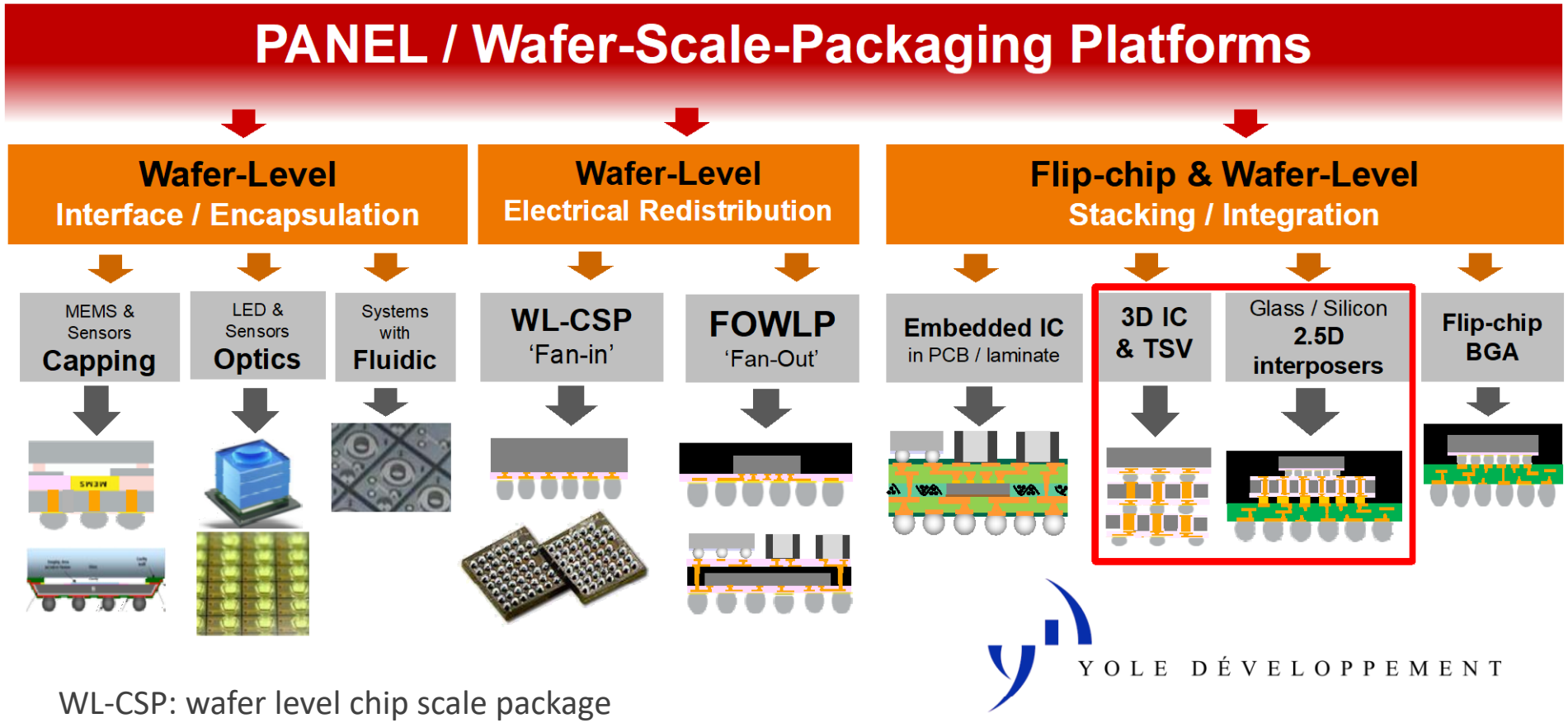


3D integration



3D integration & advanced packaging

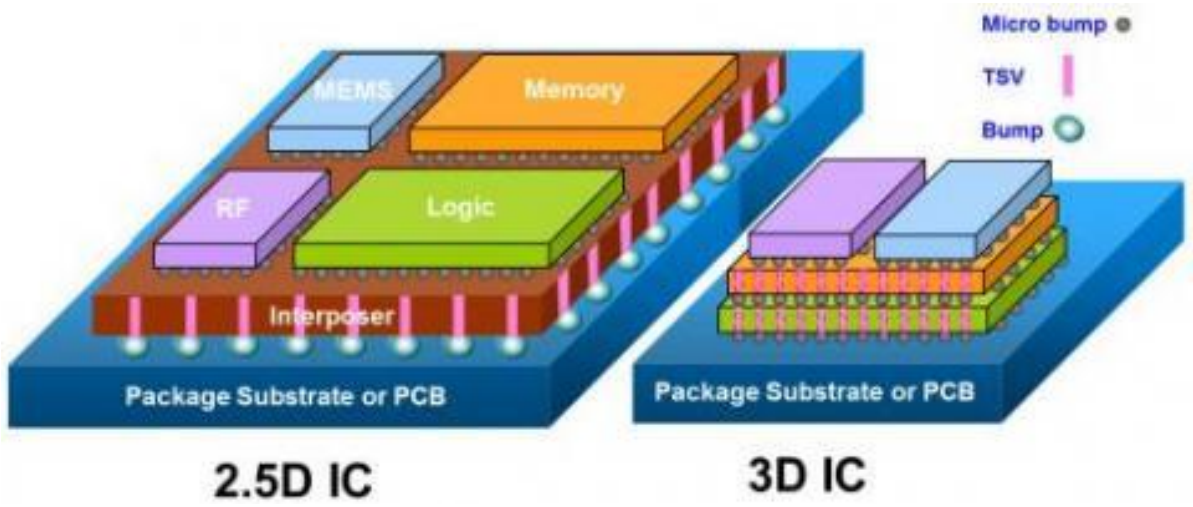
- Packaging technologies
- Many options → increased density of functionalities
- Encapsulation necessary for MEMS



WL-CSP: wafer level chip scale package
FOWLP: fan-out wafer level packaging

2.5D vs 3D integration

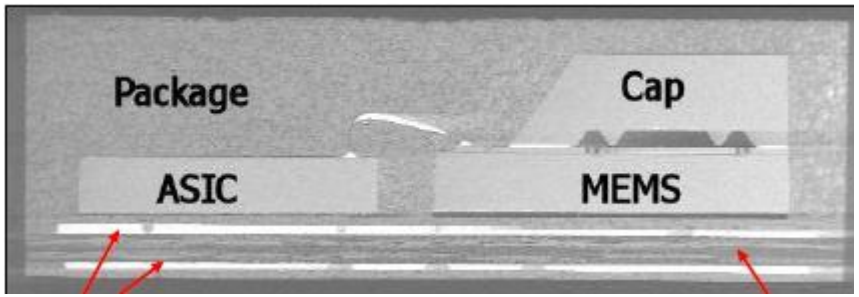
2.5D: Interposer substrate with Through Silicon Vias which function is to make the electrical link between different functional components and/or PCB-package



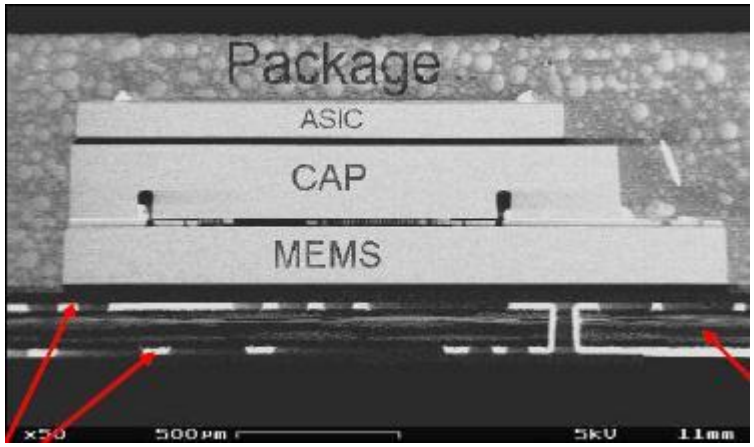
3D: Through Silicon Vias (TSVs) made directly in the functional substrate(s)

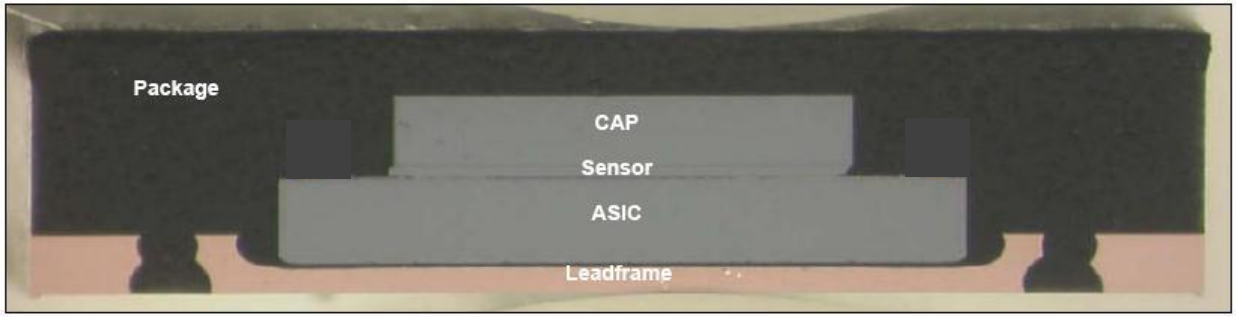
Thinning of interposer and chip is often used to reduce the length of vertical electrical (aspect ration) vias to be fabricated in the substrates.

3D Integration

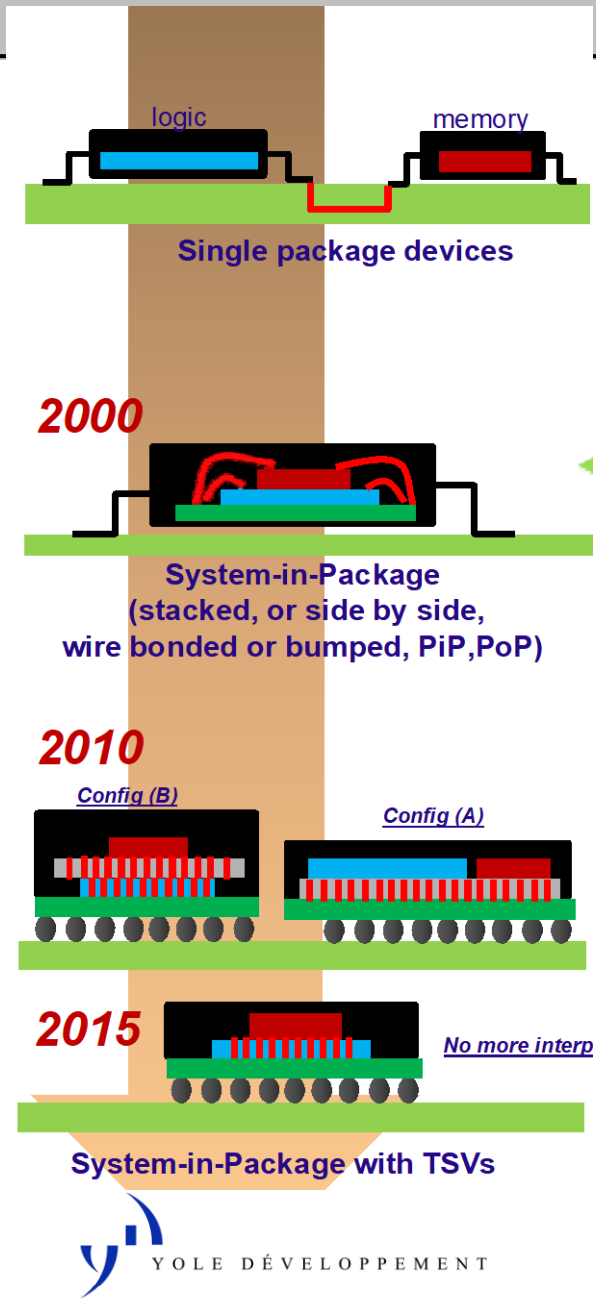


- Reduce package size
- Increase functionality
- Reduce costs





AA' Cross Section Overview

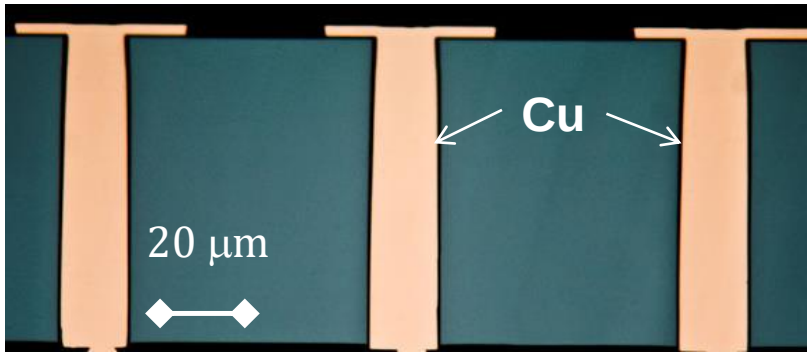


Through silicon / glass metallic vias

- R×C constant of importance
- Low noise
- Thinned interposers (glass, silicon)

For

- Reduced power consumption
- High frequency



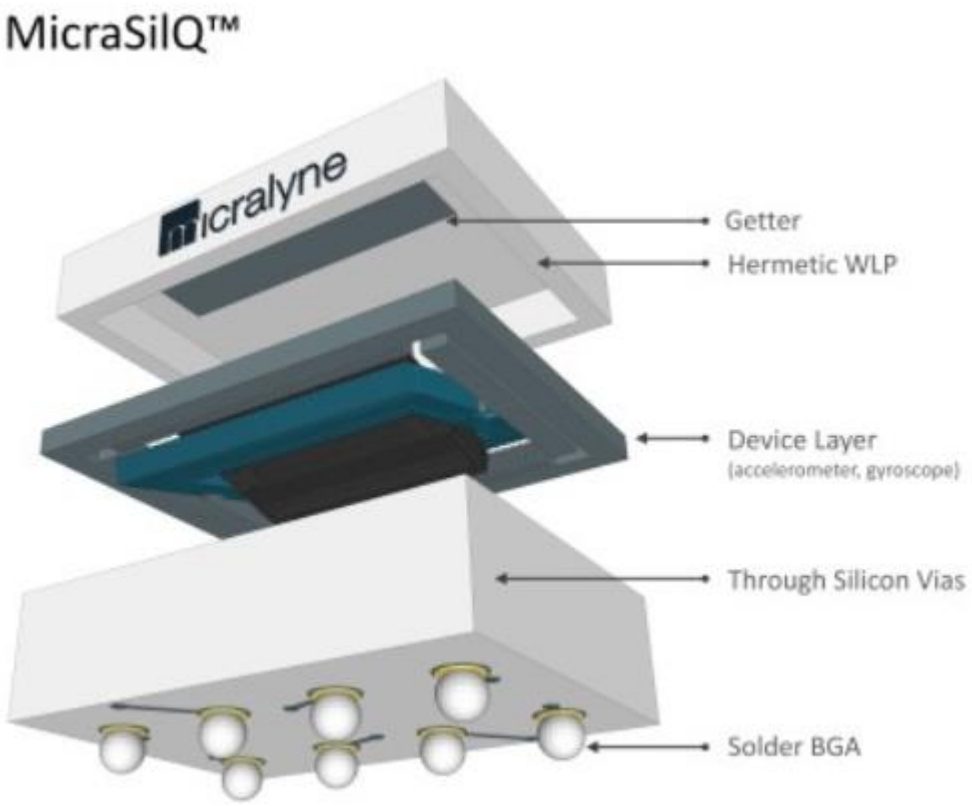
Si-interposer with Cu-TSVs
(Courtesy of Fraunhofer Institute)

General process steps

- Via drilling by Deep Reactive Ion Etching (DRIE) for Si, ultrasonic or laser drilling for Glass
- Electrical insulation if Silicon: Si oxydation, Atomic Layer Deposition-ALD of conformal Al_2O_3
- Via filling with electrical conductor: Mainly Cu using electroplating, also W, Au, conformal thin film metallisation

MEMS vacuum packaging with poly-Si TSVs

- Insulated Through Silicon Vias (TSV) – polysilicon filled
- Thick silicon device layer (60 microns standard) for high comb finger capacitance
- Lead-free solder ball grid array
- Wafer level bonding processes optimized for getter film activation and hermetic sealing

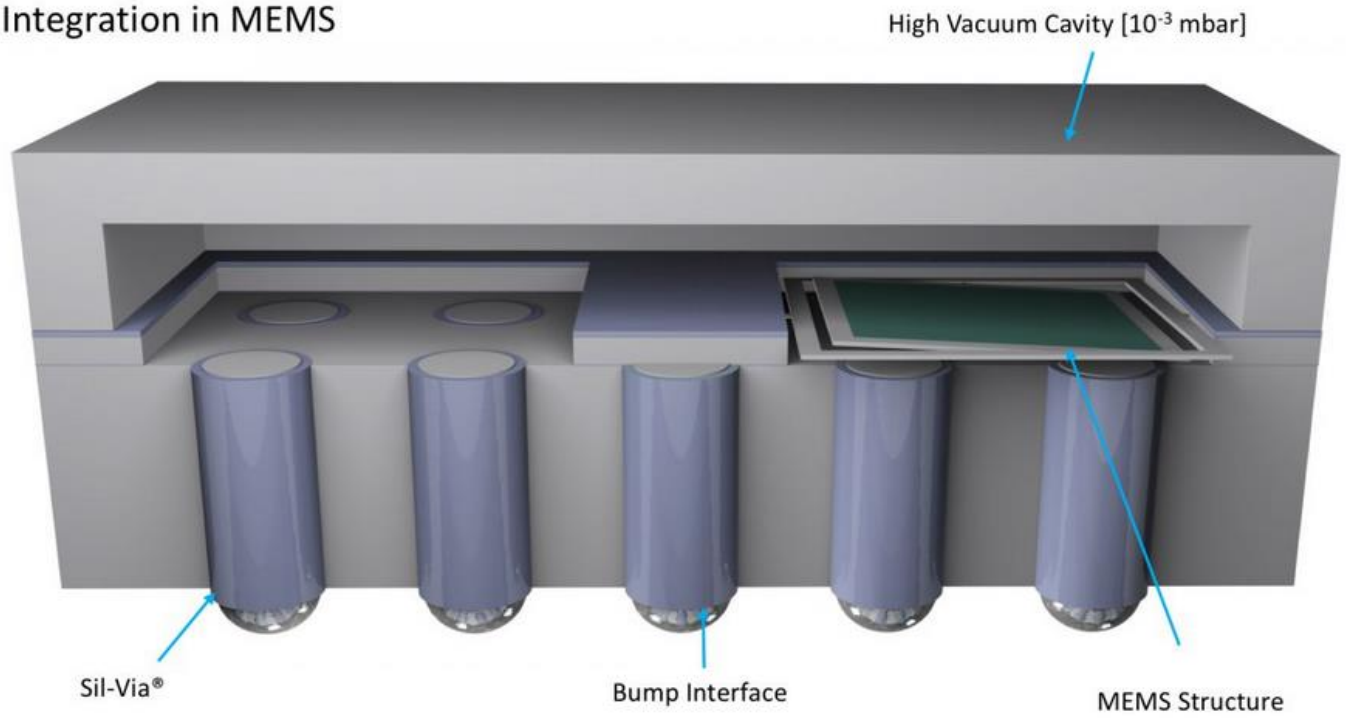


Use of silicon on insulator (SOI) wafer and surface micromachining for MEMS device fabrication

MEMS vacuum packaging with Silicon TSVs

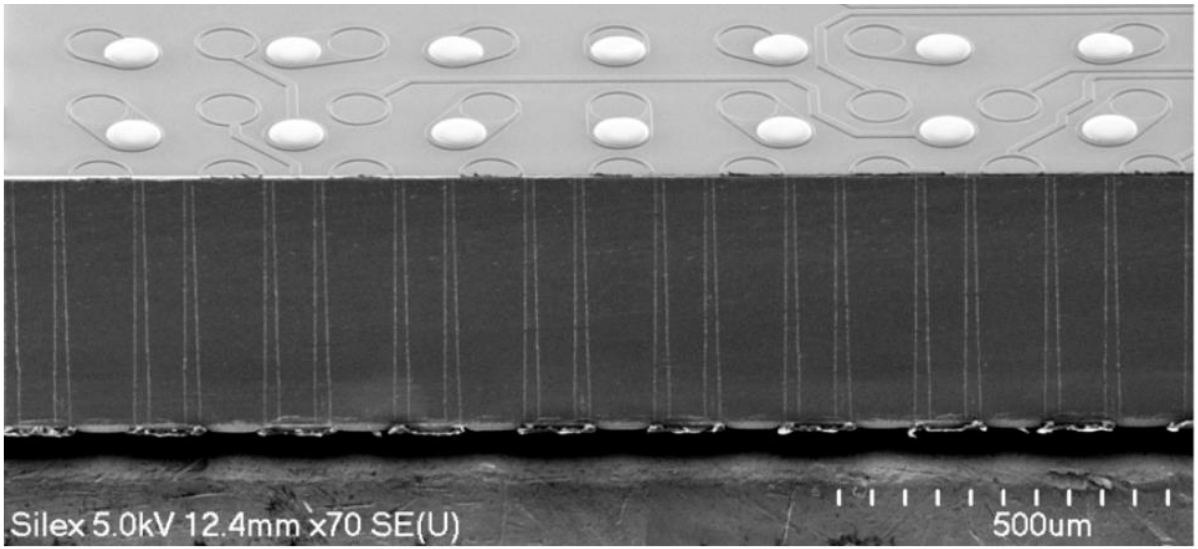
Sil-CAP® – Silex Base Technology for TSV Integration

- TSV Integration in MEMS



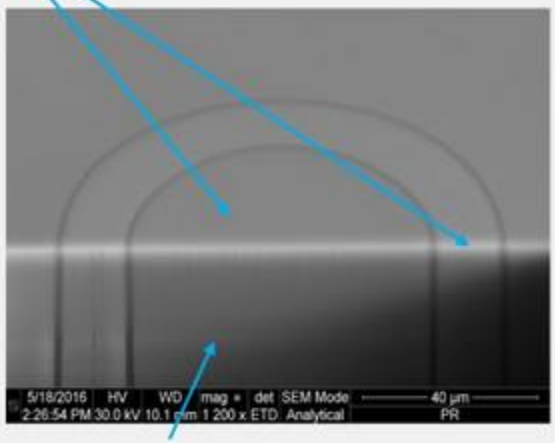
Sil-CAP® – Silex Base Technology for TSV Integration

- Patented all Silicon Through Silicon Via (TSV) in mass production since 2005
- Temperature coefficient matched vertical feedthrough for high reliability
- Hermetic, vacuum tight electrical feed through
- Any shape, maximized electrode area
- Silicon electrode, no need for metal electrode simplifies design and enables high temperature bonding an post processing



Sil-CAP® – Silex Base Technology for TSV Integration

Highly doped Si is used as starting material and separated by isolating trench



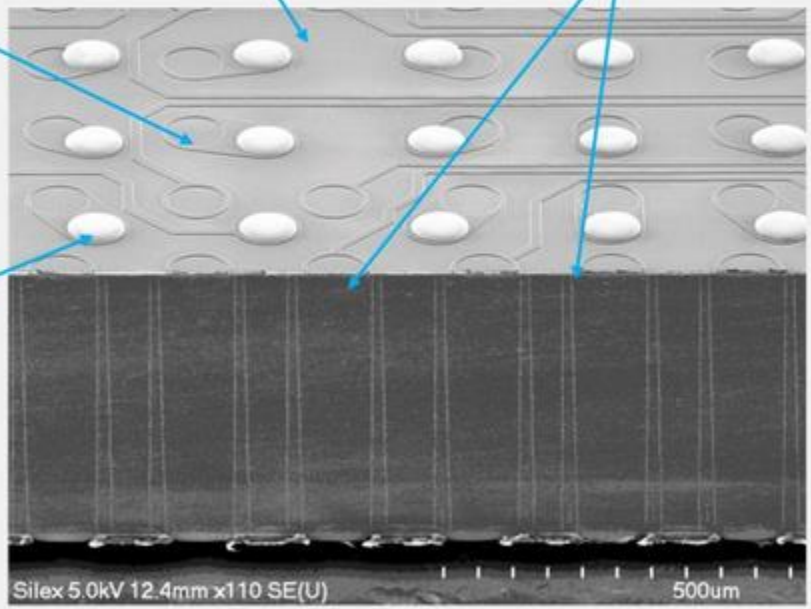
Trench isolation is >1 TΩ with breakdown voltage >1000V

Wafer thickness from 300 µm to 600 µm

UBM for Flip-chip bumping

Via pitch down to 50 µm

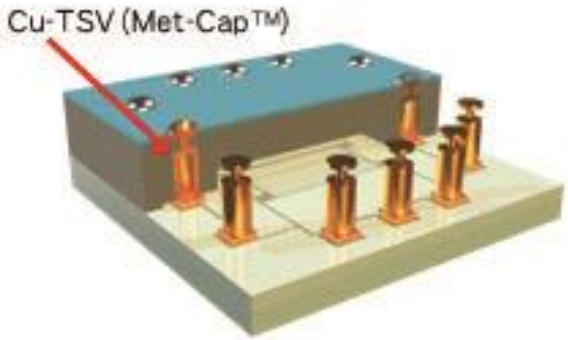
Metal routing on both sides of wafer

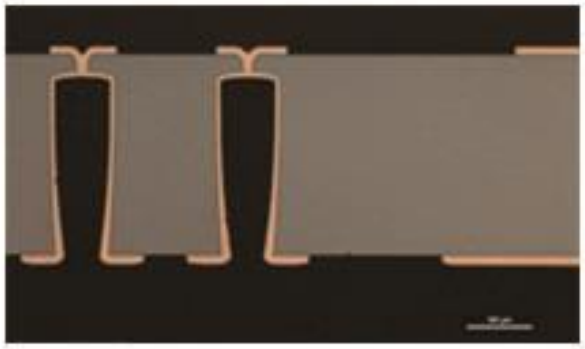


MEMS hermetic packaging with metal vias in the Cap wafer

Cu electrode TSV (Met-Cap™) from Silex

1. Fully integrated in standard building block cap wafer, may also contain a hollow
2. Perfect for RF MEMS wafer level capping
3. For 400 µm thickness, via resistance ＜25mΩ
4. 10 mTorr (Getter), 1 Torr (without Getter)
5. Yield rate >99.9%





Through glass cap vias

- **Bonded glass (interesting for RF) cap with gold or copper vias**
  - **Requires Temperature & Pressure**
  - **Surface cleaning**

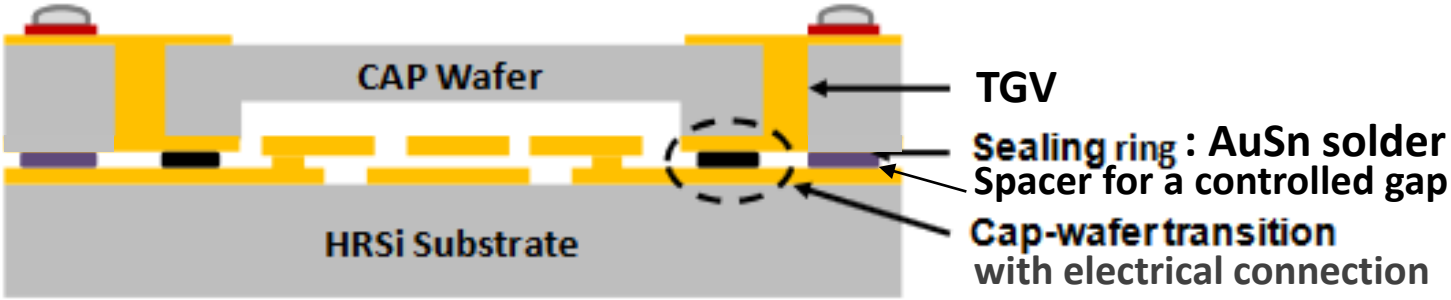


Table 1: Parameters of RF-MEMS test vehicle

Parameters	Value
Cap wafer thickness	200 µm
Sealing ring height	8-9 µm
Substrate thickness	750 µm
Substrate resistivity	1k-10kΩ.cm
Sealing ring width	200 µm

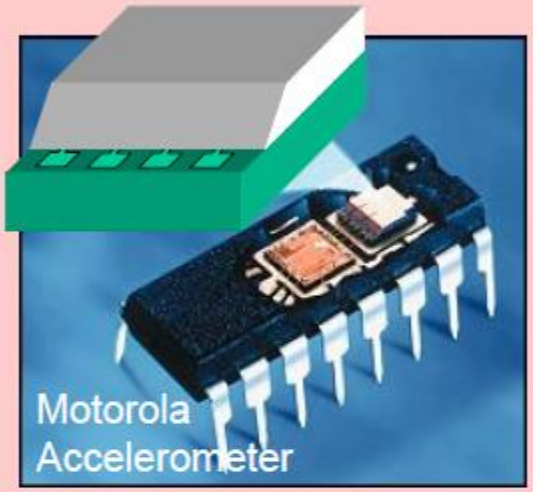
Lim et al., A broadband 3D package for RF MEMS devices utilizing through silicon vias (TSV), 16th International Solid-State Sensors, Actuators and Microsystems Conference (Transducers), IEEE 2011

Summary packaging

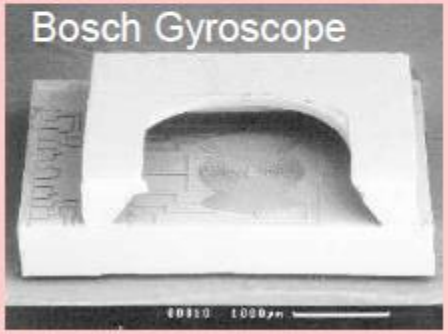
Die Level

Die level **release and** ***ceramic*** **package**

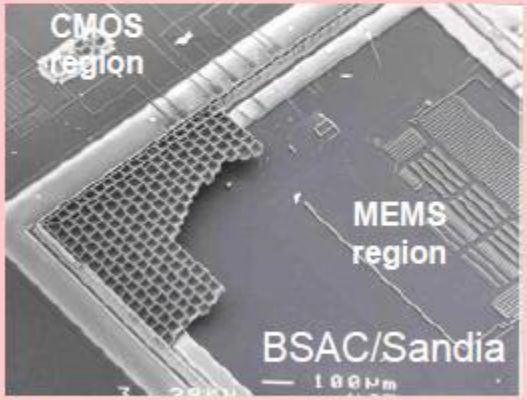
Wafer Level



Wafer bonded package with *glass frit seal* and *lateral feedthroughs* (sealed MEMS is then placed into ceramic package)

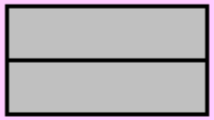
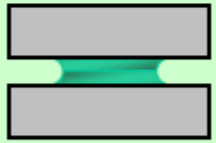
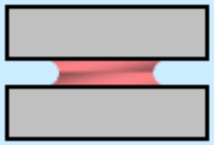


Wafer bonded package with *glass frit seal* and *lateral feedthroughs*



Partial Hexsil cap assembled onto Sandia iMEMS chip using wafer-to-wafer transfer

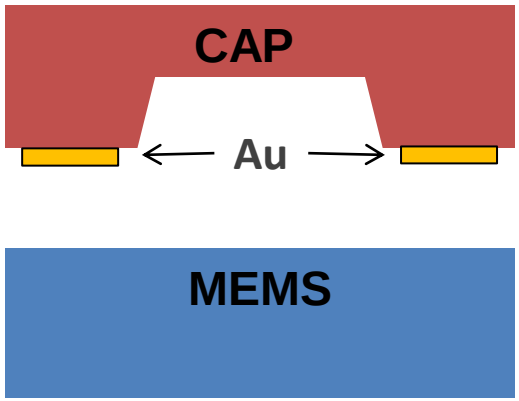
Summary packaging

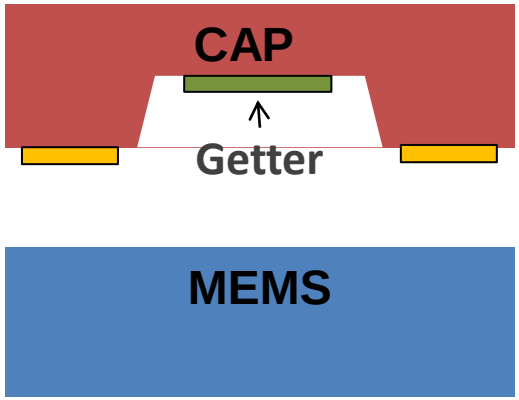
Techniques		Advantages	Drawbacks
"Surface" bonding		Hermetic	Flat surface required
	Anodic	strong bond	high-voltage
	Fusion (Direct)	strong bond	high temp
	Surface-activated	varies	varies
Metallic interlayer		Hermetic Non-flat surface ok	Specific metals required
	Eutectic	strong bond	flat surface req'd
	Thermocompression	non-flat surface ok	high force
	Solder	self-aligning	solder flow possible
Insulating interlayer		Non-flat surface ok	Varies
	Glass frit	hermetic common in MEMS	large area medium-hi temp
	Adhesive	versatile	non-hermetic

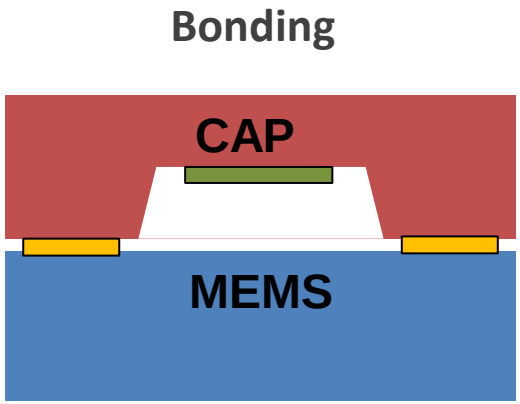
Summary packaging

Example hermetic packaging

- MEMS silicon wafer and glass Cap wafer
- Deposition of Au thin film bonding layer for eutectic bonding on Cap wafer
- Deposition of thin film getter layer in cap wafer
- Pump down the bonding chamber
- Apply pressure and temperature (400°C) for Au-Si eutectic bonding
- Getter film is activated during bonding process







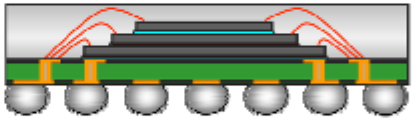
Summary packaging

Packaging world

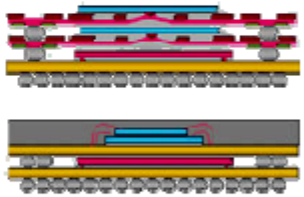
Need for more compact systems

Need 3rd dimension to reduce packaging cost & dimension

Chip level 3D solution



Stacked dice



Package on package

2.5D TSVs interposer or 3D TSVs directly drilled in functional substrate

Summary packaging

- One general statement about MEMS packaging

  « One MEMS = One packaging »

- Packaging is typically the major part of the cost of microsystems (up to 70-80% of the total cost)

- Standardisation is one of the main actual issues

- Wafer level packaging solutions are more and more proposed

- 3D-integration based on through silicon vias is emerging

Questions

- Packaging
  - Packaging levels
  - Packaging process: materials, processing steps, types of packages
  - Difference between IC and MEMS packaging
  - Die vs wafer level packaging
  - Packaging of physical sensors, chemical sensors
  - Applications of adhesive bonding
  - Reliability issues

- Hermetic packaging
  - How to get hermetic packaging (materials, bonding techniques and getters)
  - Gas sources for hermetic packaging
  - Bonding / sealing techniques, advantages & disadvantages
  - Vacuum requirements for different MEMS
  - Characterisation of gas leakage in hermetic packaging

- 3D integration
  - Why 3D integration and advantages of using TSVs
  - 2.5D vs. 3D integration
  - Through silicon vias vs. lateral feedthrough
  - TSVs fabrication
  - System in package vs. system in package with TSVs